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WAFER PROBE AND COPPER PILLARS: CHALLENGES AND SOLUTIONS

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The copper pillar bump process—once restricted to specialized high-end microprocessors—is finding increasing acceptance in a variety of system-on-a-chip devices employed in mobile electronics such as smart phones and tablets.

Functioning as a die-to-package interconnect, copper pillars help reduce packaging costs, boost device I/O density and performance and offer thermal control benefits.

The materials and increased probe densities (i.e., decreased probe-to-probe spacing) associated with this novel packaging technology, however, present considerable challenges to conventional wafer probe tooling and processes.

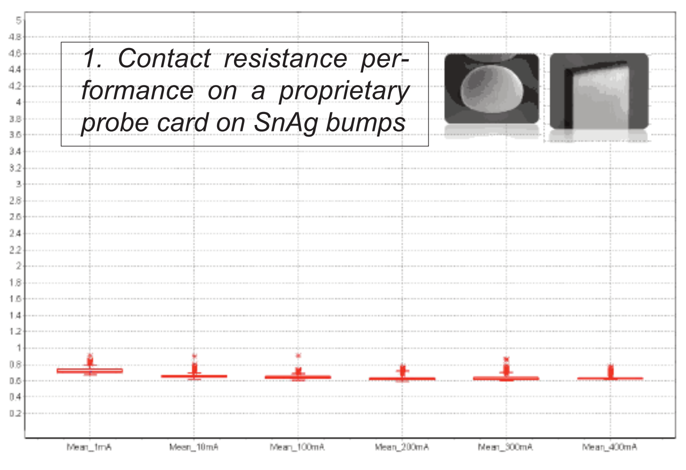
Meeting Probe Card Performance Demands

This article highlights these challenges and proposes a probe card architecture that meets performance requirements.

Copper pillars help reduce packaging costs, boost device I/O density and performance and offer thermal control benefits.

It also provides the flexibility to meet the increasing number of material and layout combinations used in the mobile SoC packages of today and in the future cost-effectively.

WAFER PROBE & COPPER PILLARS



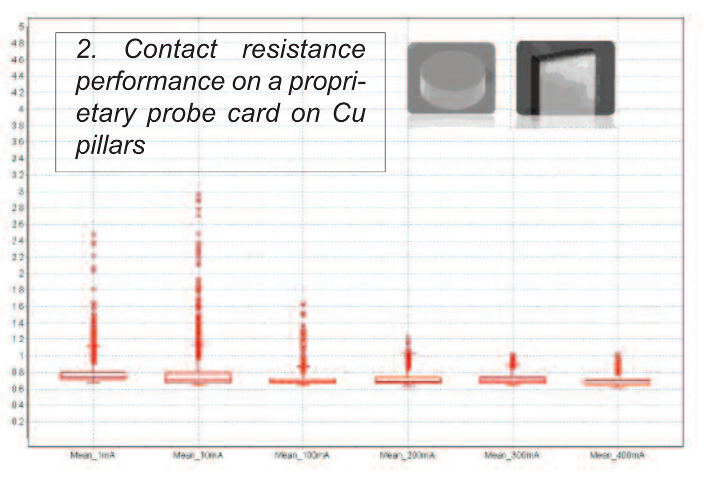
1. Contact resistance performance on a proprietary probe card on SnAg bumps

A Change from Tradition

Traditionally, package interconnects have used eutectic solder balls in flip-chip applications or aluminum pads in wire-bond applications.

Accordingly, traditional probe technologies have been optimized to ensure good electrical and mechanical compatibility with those metallurgies during wafer test.

Adoption of tin-silver solder balls for lead-free, flip-chip packaging processes have demanded some moderate changes in probing processes and probe-card architectures; however, the rapid oxidation of copper requires some additional approaches to ensure stable contact resistance during wafer probe of copper-pillar-bumped devices.



2. Contact resistance performance on a proprietary probe card on Cu pillars

Contact Resistance

As shown in Figures 1 and 2, a probe which provides good contact resistance performance on SnAg solder bumps fails to provide the same level of performance on copper pillars, most significantly at lower current levels.

Failure to achieve a stable contact resistance (below approximately 2 ohms in this test setup) will result in reduced device yields, with a corresponding loss in overall factory throughput and efficiency purely because of inferior probe-card performance.

In addition, since a probe card technology deployed to test a copper-pillar-bumped device may be required to probe on either bare copper or tin/solder- capped copper, a flexible architecture that can be used in both situations with a minimum of changes would be advantageous.

Material-Driven Probing Challenges

These material-driven probing challenges are magnified when coupled with the relentless increase in I/O density, and the corresponding decrease in probe-to-probe spacing (pitch).

One of the key advantages of copper-pillar interconnects is the increased density compared to that available from solder-ball interconnects.

However, the mechanical precision and accuracy required to reliably contact these interconnect arrays makes it extremely challenging to address sub-130μm pitches on full-grid-arrays with traditional mechanically-formed probe structures.

Solutions to this geometrical scaling challenge have been deployed, with most probe card manufacturers relying on various semiconductor-based “micromachining” or MEMS processes using sub-micron-capable lithography and etch processes.

Probe Shapes and Structures

When combined with a sufficiently broad material set, a MEMS process can produce a variety of probe shapes and structures, allowing the probe card manufacturer to optimize a probe design for a particular application.

An example of the results of such a material and geometry optimization for copper pillar applications is shown in Figure 3, which illustrates a significant contact resistance performance improvement over Figure 2.

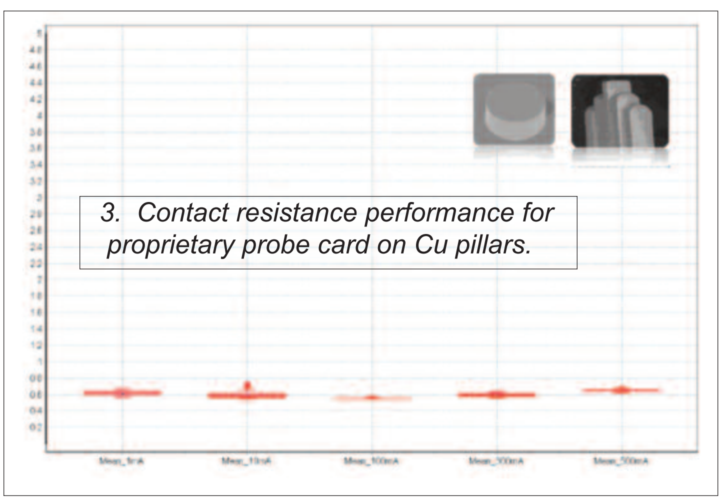
Unacceptable Contact Resistance on SnAg

Interestingly, as shown in Figure 3, the probe optimized for copper-pillar applications demonstrates unacceptable contact-resistance performance on SnAg bumps.

Therefore, it would seem that a different probe material and geometry is required to successfully meet the performance requirements on both copper pillars and tin-silver solder balls.

Given this constraint, it is then advantageous to be able to perform this probe-level optimization with a minimum of change to the rest of the probe card.

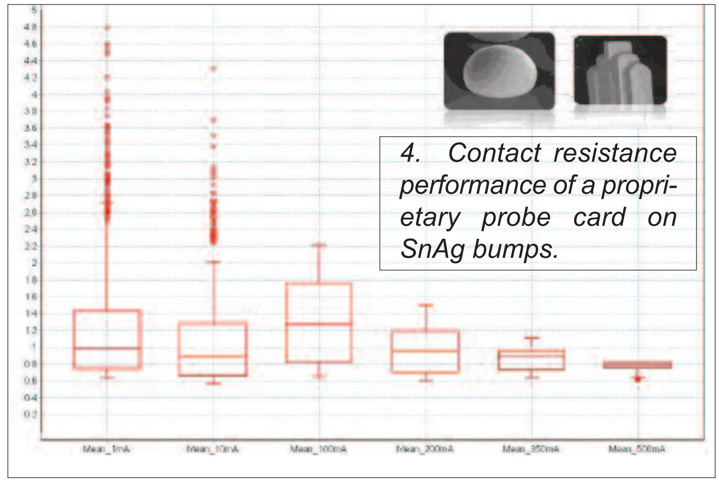
As the diversity of packaging technologies continues to flourish with emerging applications such as embedded Wafer-Level Packaging (eWLP) and Through Silicon Vias (TSVs), the probe-level flexibility shown in Figure 5 will become increasingly useful.



3. Contact resistance performance for proprietary probe card on Cu pillars.

Conclusion

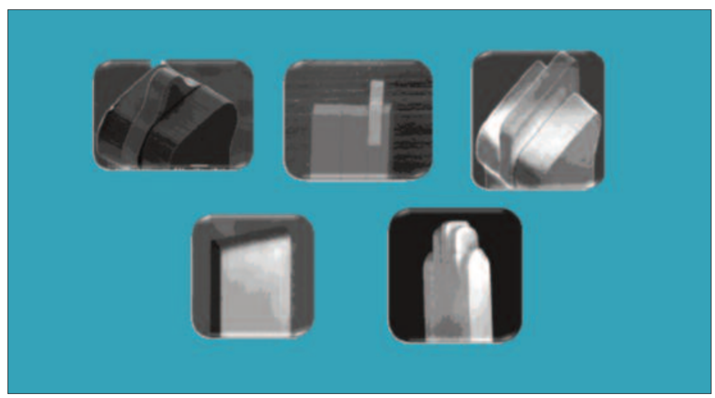
Copper-pillar bump technology, which is increasingly being used in an array of SoC packages for mobile applications, has outstripped the capability of classical probe card technologies due to shrinking pitches and the introduction of copper to the probing process.



4. Contact resistance performance of a proprietary probe card on SnAg bumps.

While MEMS probe cards can address the requirements for increased probe density, MEMS alone does not provide the flexibility to easily optimize probe cards for the increasing diversity of packaging materials and layouts.

The technology described not only meets today's requirements for copper pillar probing, but also those of other emerging packaging technologies such as eWLP and TSVs.



5. Probe-level flexibility will become increasingly useful with emerging applications.

Dr. Slessor has served as president and CEO of MicroProbe since July 2008.

He received a Ph. D. in aeronautics and physics from Caltech, Pasadena, Calif., and a B.A.Sc. in engineering physics from the University of British Columbia. Contact him at mslessor@microprobe.com.

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