# Advanced Technique for Broadband On-Wafer RF Device Characterization

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***Abstract* – A technique for a broadband 2-port on-wafer RF device characterization is presented. It utilizes advanced LRM+ calibration with standards realized on a Si wafer. The approach relies on three standards: a non-perfect Thru standard, a reflection standard which is symmetrical for both ports and a complex match (Load) standard which can be different for both ports. Models for such kind of standards as well as LRM+ calibration are not supported by currently available VNA firmware. The presented method allows to set up a planar customized calibration kit (e.g. on a Si wafer) which has the same contact pad design as used for an on-wafer DUT. A simple procedure to compensate different DC resistances of port-to-port and set-to-set variation for on-wafer realized Load standards is shown. Additional wafer embedded verification elements as well as real DUT measurement results were used to compare the accuracy of the new method with the state of the art calibration and de-embedding procedure. A good calibration accuracy and significant simplification of RF device characterization procedure has been achieved with the proposed approach.**

## I. INTRODUCTION

On-wafer 2-port S-parameter measurements are used to characterize the RF behavior of active and passive semiconductor devices. To achieve the necessary measurement accuracy all modern vector network analyzers (VNA) support different calibration procedures [1]. Due to these procedures the systematic errors of the measurements (e.g. imperfection of directional couplers, cable, adapter and wafer probe influences etc.) can be determined and subtracted from the measured values. In advanced RF technologies the dimensions of on-silicon active devices get smaller. Because of this the transient time is decreased and consequently the cut off frequency and power gain at high frequencies are increased. The junction capacitances of SiGe:C HBTs in the IHP technology [2] are in the range of 3 fF. For on-wafer measurements of such devices, additional de-embedding procedures are commonly used to obtain the properties of intrinsic devices without the contact pad parasitic. Different de-embedding procedures are known [3], [4]. Typically a 3-step de-embedding method [3] (using Open, two Shorts and a Thru dummy) is recommended for frequencies higher than 40 GHz.

In this paper, an accurate approach for on-wafer calibration is introduced that does not require de-embedding of the DUT contact pads. The approach relies on advanced LRM+ calibration, performed with customized wafer-embedded calibration standards, implemented on a SiGe:C wafer. The description of the calibration procedure is given in the next section. The design of the wafer-embedded calibration standard as well as the modeling and the electrical description of standards are discussed in the third section. The on-wafer LRM+ calibration was performed with frequencies up to 110 GHz. The verification results of the calibration accuracy are presented in section four. The measurement results of the real DUT with the conventional method (calibration on alumina and additional de-embedded) and the new advanced technique are included in section five. The comparison of both experimental results proves that the proposed technique provides high measurement accuracy. In addition it simplifies the calibration procedure of the measurement system significantly.

## II. CALIBRATION OF THE MEASUREMENT SYSTEM

A broadband VNA typically realizes a 4-receiver architecture (two reference and two measurement channels). In Fig. 1 a physical model of the systematic errors for a 4-receiver VNA is shown. In this figure *[Tx]* is a measured DUT; *[A]* and *[B]* are unknown 2-ports, that describe measurement systematic errors ("error boxes"); $m_1 \ldots m_4$ are values, measured by idealized receivers.

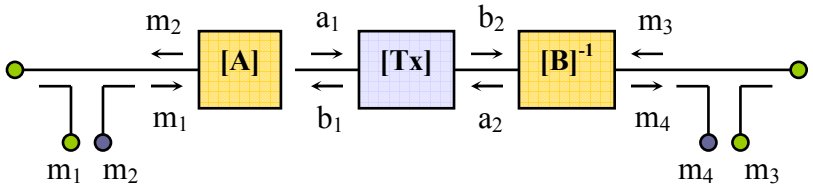



Fig. 1: Physical error model for a 4-receiver VNA

It is easy to show that the relationship between measured $m_1 \ldots m_4$, incident ($a_1$, $a_2$), reflected/ transmitted ($b_1$, $b_2$) signals is:

$$\begin{pmatrix} m_1' & m_1'' \\ m_2' & m_2'' \end{pmatrix} = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \begin{pmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{pmatrix}^{-1} \begin{pmatrix} m_3' & m_3'' \\ m_4' & m_4'' \end{pmatrix}, \quad (1)$$

where: $m_1' \ldots m_4'$ and $m_1'' \ldots m_4''$ represent the measured values in forward and reverse directions correspondently; $T_{11} \ldots T_{22}$ – transmission parameters of a measured DUT. Alternatively, in shorted form:

$$M = ATB^{-1}, \quad (2)$$

where measurement matrix $M$ is:

$$M = \begin{pmatrix} m_1' & m_1'' \\ m_2' & m_2'' \end{pmatrix} \begin{pmatrix} m_3' & m_3'' \\ m_4' & m_4'' \end{pmatrix}^{-1}. \quad (3)$$

The calibration procedure (definition of matrices *[A]* and *[B]*) can be performed by measuring three different standards $N_1$, $N_2$, and $N_3$:

$$M_i = AN_iB^{-1}, \qquad (i = 1 \ldots 3). \quad (4)$$

To characterize the system (1) completely, only 7 unknowns have to be found from 12 equations yielded from (4). This redundancy sets general requirements to the calibration standards, presented in Table I.

TABLE I

GENERAL REQUIREMENTS FOR THE CALIBRATION STANDARDS

| Standard | Requirements |
|---|---|
| $N_1$ | 4 known parameters (fully known) |
| $N_2$ | Minimum 2 known parameters |
| $N_3$ | Minimum 1 known parameter |

Different calibration procedures can be derived according to these requirements [5]. We analyzed commonly used procedures (conventional [6] and multi-line TRL [9], conventional [11] and modified LRM [12, 13], LRRM [14, 16]) with regard to the customized kit and the needs of broadband calibration on silicon wafers. Popular SOLT calibration [17, 19] and its modification [18] were considered as well. According to [21] none of these methods can be applied because of the following reasons:

- realization of the long calibration lines is problematical
- accurate characterization of customized Open and Short standards in a wide frequency range is complicated [7]
- frequency dependency of the Load standard [8, 10, 13]
- Load cannot be trimmed to an ideal 50 Ohm DC resistance
- DC resistance of the Load pair for port 1 and port 2 can be different

On the other hand, the advanced LRM+[1] calibration [22] relies on known 2-port Thru standard (*N1*), two known Load (Match) standards (represented by *N2*), and two partly known reflections (*N3*). The following properties of standards *N2* and *N3* can be noted for the on-wafer application of advanced LRM+ calibration:

- reflection should be known only within ±180 degree (close to Open or Short)
- on-wafer reflection standard should be free from in-pair asymmetry
- typically realized in-pair, Match (Load) standard can be different from each other and can be represented by any known arbitrary impedances

Summarizing this discussion, we can say that the LRM+ procedure meets our requirements better than any other method. It is self-consistent; the on-wafer calibration kit is easy to realize (for semi-insulation as well as for conductive substrates); it accumulates only three standards, saving the wafer space, it is not sensitive to the Load standard DC and RF variation and ports symmetry [22], and it does not require the wafer probes replacement.

## III. Design of the On-wafer LRM+ Calibration Kit

### *A. Design of Calibration Standards*

A set of three standards was designed for the on-wafer calibration method. It consists of Thru, a pair of Load, and a pair of Short standards (Fig. 2b, 2c, 2d). The reference plane is set in a way that most HBTs fit perfectly in the gap. All standards are designed as wide as possible to reduce the skin effect. An Open structure (Fig. 3c) and an Attenuator (Fig. 3d) were added to the test suite for on-wafer accuracy verification tasks. The structures in Fig. 3a and Fig. 3b are used for the 3-step de-embedding.

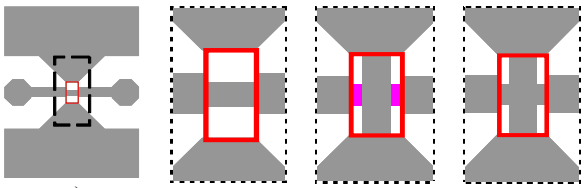



Fig. 2: Wafer embedded LRM+ calibration kit: a) Thru; Zoomed views: b) Thru, c) Load, d) Short; Red box shows the calibration reference plane.

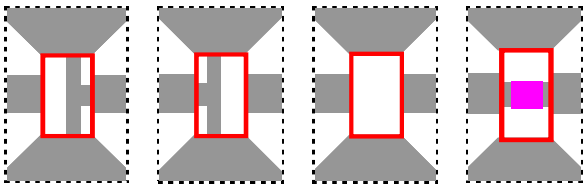



Fig. 3: De-embedded dummies (zoomed view): a) Open-Short, b) Short-Open; verification elements: c) Open, d) Attenuator; Red box shows the de-embedding reference plane.

### *B. EM Simulation*

The RF behavior of the non-ideal Load and Thru are determined using ADS Momentum EM-simulation tool of Agilent. In the simulation only the parts inside the reference plane were taken into account. The lossy behavior of the silicon substrate is respected. The mismatch between the load structures due to process variations was also considered. The results are sets of S-parameters. They form the base for the later definition of the calibration standards.

[1] LRM+ calibration is implemented in commercially available VNA calibration software SussCal® 5.1 from SUSS MicroTec.

*C. Modeling of the Load Standard*

DC measurements were performed to get data for the mismatch between the Load standards. Table II shows the results. The contact resistance is already subtracted. It was not possible to used Kelvin probes since the contact pads are too small for them. The Load resistances vary in a range of 49.8 Ohm to 51.5 Ohm.

TABLE II

VARIATION OF THE LOAD RESISTANCE

| **Die** | **C314** | **C311** | **C36** | **C87** | **C710** |
|---|---|---|---|---|---|
| **$R_1$, Ohm** | 50.89 | 51.25 | 50.64 | 50.58 | 51.45 |
| **$R_2$, Ohm** | 50.38 | 50.56 | 50.82 | 49.76 | 50.63 |

| | $\overset{\circ}{R}_{mean}$, **Ohm** |
|---|---|
| Port 1 | 0.82 |
| Port 2 | 0.43 |

The different widths of the Load standards are derived from the experimental data. These structures were then simulated with Momentum. The sheet resistance was not changed for the different simulation runs. For the Load modeling it is important to know, whether the RF behavior changes with different Load dimensions or not. The simulation results (S-parameters) were transformed to Z-parameters to investigate this fact. The Load resistance of each port is extracted as real part of the Z-parameters and normalized to the value at the lowest frequency $f_0$ (5).

$$R_{norm}(f) = \frac{\Re\left(Z_{xx}(f) - Z_{yx}(f)\right)}{\Re\left(Z_{xx}(f_0) - Z_{yx}(f_0)\right)}; x, y = 1..2; x \neq y \tag{5}$$

Fig. 5 shows the normalized real parts of the minimal and maximal Load as a function of frequency. As expected it increases with the frequency due to the skin effect. The average of both curves is calculated and fitted as a second order polynomial (6).

$$R_{normfit}(f) = 4.8757 \cdot 10^{-25} \cdot f^2 + 3.11 \cdot 10^{-14} \cdot f + 1 \tag{6}$$

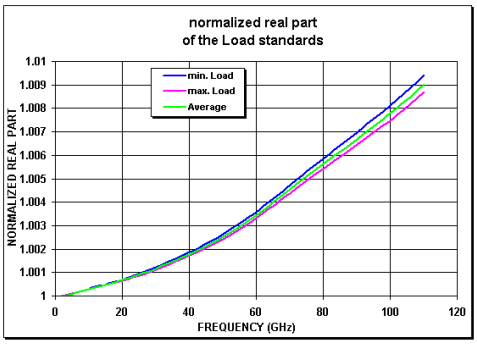



Fig. 5: Normalized resistance of the slightly different models used for LRM+

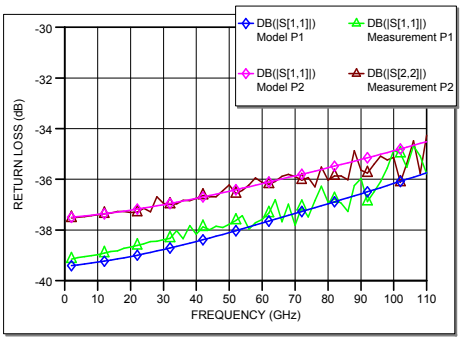



Fig.6: Load standard used for LRM+ calibration: models and measurement results

The imaginary part was also extracted from the simulated data. Normalization was not performed since it is not necessary as shown later. The average per frequency is stored in a lookup table IM. This table is used to describe the imaginary part of all Load standards. The determination of the normalized real part and the imaginary part has to be done only once, but it has to be repeated if the design of the load standards has changed.

The RF behavior of the Load standards is known now, but with a normalized real part. During calibration it has to become an absolute value again. This is done by two DC measurements before the actual calibration. The first DC measurement is performed with the Short standard to get the ohmic losses of the bias tees and the contact resistance. The next step is to determine the DC resistances of the Loads

later used for on-wafer calibration corrected by the ohmic losses and contact resistances. With the measured Load resistance and the now known RF behavior a complex Load model is built (7).

$$Z_{LOAD,X}(f) = R_{DC,X} \cdot R_{normfit}(f) + j \cdot IM(f)$$
$$S_{XX}(f) = \frac{Z_{LOAD,X}(f) - Z_0}{Z_{LOAD,X}(f) + Z_0}$$
$$x = 1..2 \qquad (7)$$

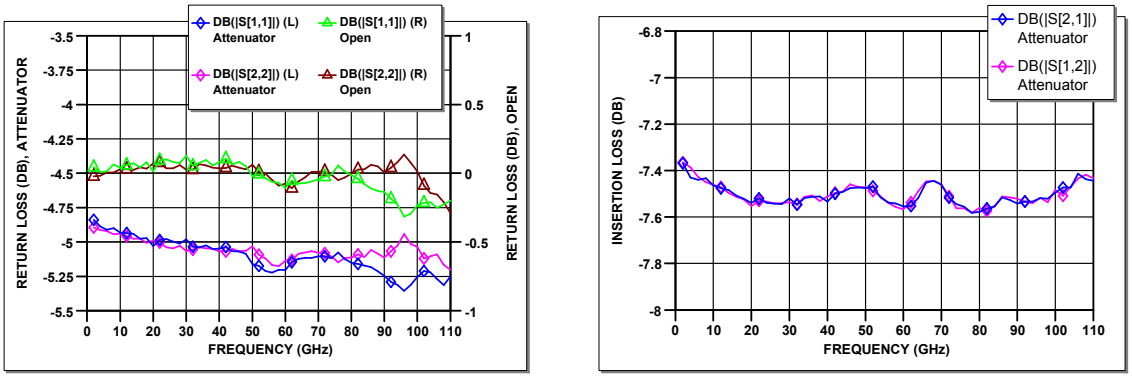
The complex Load behaviors are now converted into S-parameters and stored as TouchStone files (one for each port). The calibration software SussCal 5.1® takes these files of the Load definitions for the LRM+ calibration.

The Load standard models used for the LRM+ calibration are shown in Fig 6. Load port 1 (series "Model P1") is different from Load port 2 (series "Model P2"). The value of the model "offset" depends on the DC resistance of both Loads. The loads were re-measured after the calibration and afterwards compared to the defined models. Measured results show very good congruency with the defined models in general. However, a small difference of about 0.27 dB for the port 1 data at low frequencies can be recognized. It is presumed, that the difference is caused by a lack of contact on the port 2 during the measurement tests.

## IV. Verification of the On-wafer LRM+ Calibration

There are different techniques for the calibration accuracy verification. However, none of them can be applied for lossy wafers (Si, SiGe etc). We excluded those, based on the measurements of long transmission lines: commonly used "ripple test" and methods from [20]. As far as LRM+ calibration relies on only one reflection standard (Open or Short), the second one can be successfully used for the accuracy verification. We have selected Short standard (Fig. 2, d) for the on-wafer LRM+ calibration and Open (Fig. 3, c) for the verification purpose (Fig. 7, a). With the help of the second verification element (Attenuator, Fig. 3, d) we have also tested the accuracy of the reflection (Fig. 7, a) as well as the transmission measurements (Fig. 7, b). By definition, both verification elements have unknown electrical behavior but symmetry for port 1 and port 2. Thus we can qualitatively verify the calibration accuracy.

It is well known, that the Load standard defines the reference impedance of the measurement system in LRM-like calibration methods [11-14]. However, the planar on-wafer Load is realized in pair (Fig 2, c). As it is mentioned in [21], [22], the asymmetry between Load port 1 and Load port 2 (for instance caused by wafer fabrication) affects the reference impedance definition. Results demonstrated on the Fig. 7 proves, that the forward and reverse return loss measurements of the Open and Attenuator as well as insertion loss of the Attenuator are very symmetrical. Hence, the LRM+ algorithm has accurately compensated for the Load pair asymmetries, demonstrated in section II.




a) b)

Fig. 7: Verification results of the of on-wafer LRM+ calibration:
a) Reflection measurements of the Open and Attenuator structures
b) Transmission measurements of the Attenuator structure

However, an "unsymmetrical zone" for the return loss measurements between 80 GHz and 105 GHz with the maximum error at 96 GHz of ±0.2 dB for Attenuator and ±0.22 dB for Open element correspondently can be found. The calibration error of ±0.2 dB is typically acceptable in practice for this frequency range. We suppose that the mentioned effect was caused by the unsuspected simulation error of the RF part of the Load standard model and has to be investigated in the future.

We have also re-measured the Thru standard (Fig. 2, a, b) after the on-wafer LRM+ calibration and compared the results with the EM simulation. The comparison of the results shows very good fitting as well (Fig. 8).

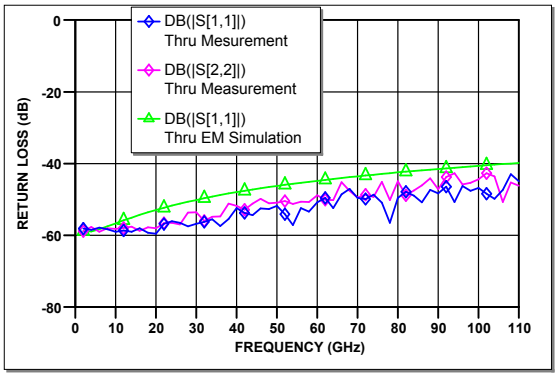



Fig. 8: Return loss of the wafer-embedded Thru standard: EM simulation results and the verification measurements after the on-wafer LRM+ calibration

## V. Measurement Results of the Active DUT

For comparison the cut-off frequency of a HBT was measured in a conventional way (calibration on alumina and further DUT contact pads de-embedding) and proposed on-wafer LRM+ calibration method. The HBT was also measured with an off-wafer (on alumina only) LRM+ calibration. We used a 3-step de-embedding procedure to compensate for the influence of DUT pads [3]. The reference plane after de-embedding is at the same position as after on-wafer calibration. Only under these circumstances the results can be compared with each other. Fig. 3 shows additional dummy structures used for de-embedding. The results are shown in Fig. 9. The non de-embedded data (green curve) gives a lower cut-off frequency due to the influence of pad parasitic. The congruence between the on-wafer LRM+ calibration and the off-wafer (on alumina) calibration together with de-embedding is very good.

The experiments were performed using an Agilent 8510XF network analyzer, semiautomatic wafer probe system PA200HF, and calibration software SussCal® 5.1 from SUSS MicroTec (Fig. 10).

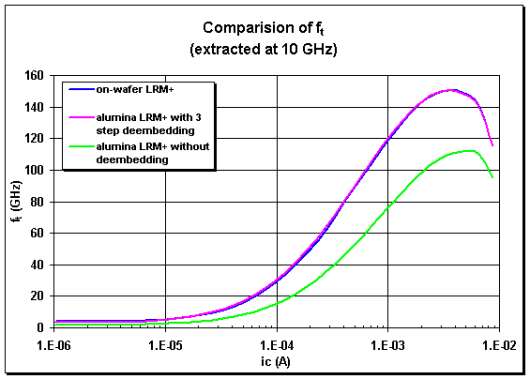



Fig. 9: Cut off frequency $f_T$ vesus collector current ic of a SiGe:C HBT

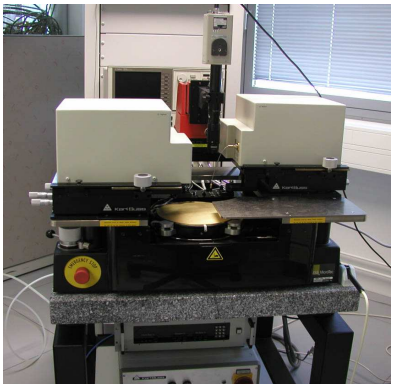


Fig. 10: The measurement system used for the experiment

## VI. Conclusion

We demonstrated that the presented technique based on the LRM+ calibration provides very good measurement accuracy, compared with the conventional way of calibration on alumina, requiring additional pad de-embedding. Moreover, it reduces the number of required reference elements (dummies or standards) as well as measurement steps (from 8 to only 4), and minimizes a typical measurement error (e.g. due to bad contacting on silicon). It can be successfully used for reliable broadband on-wafer RF device characterization, especially on highly lossy material like a silicon wafer.

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