SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

Fully Automated Integrated Silicon Photonic Wafer Test

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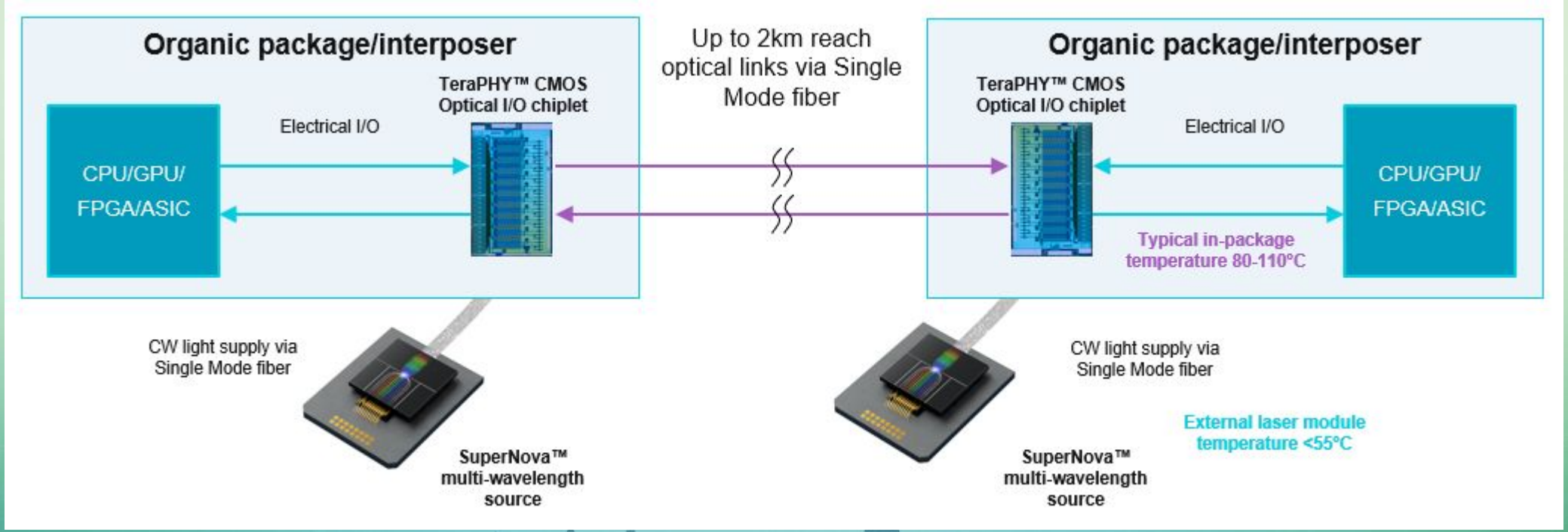
Overview

- Introduction to Ayar Labs
- Early Characterization Setup
- FormFactor CM300-Silicon Photonics Probe Station
  - Overview of Test Executor
  - Improving Test Throughput
- Improved Test Flow
- Current Work: Low Loss Wafer Level Edge Coupling
- Future Work: Probe Card for Wafer Level Electrical-Optical Probing for KGD

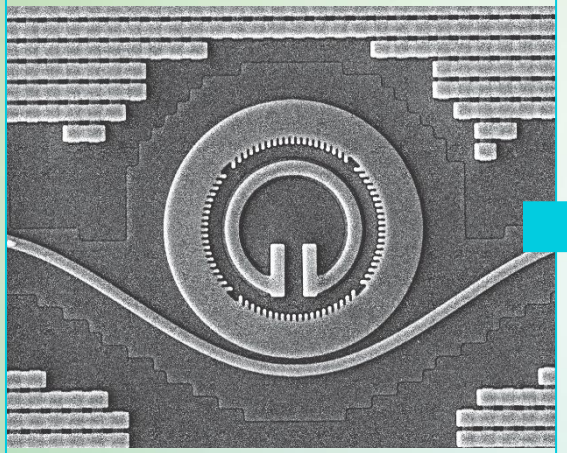
Introduction

- **Ayar Labs develops monolithic optical I/O chiplets (TeraPHY™) to enable high bandwidth, low latency, and low power consumption interconnects for chip-to-chip communication**
- **Applications**
  - High performance computing
  - Disaggregated memory/compute architectures



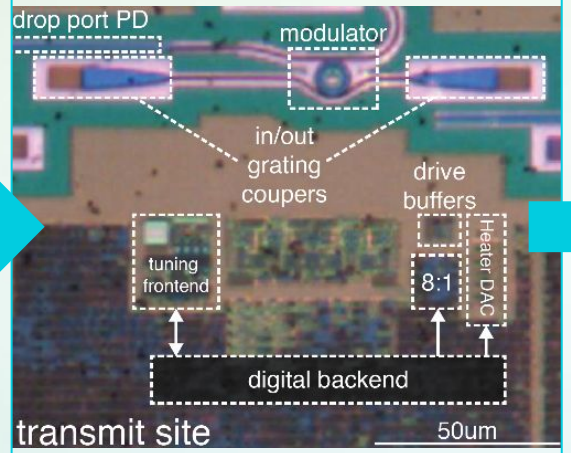
Technology

Micro-ring Resonators



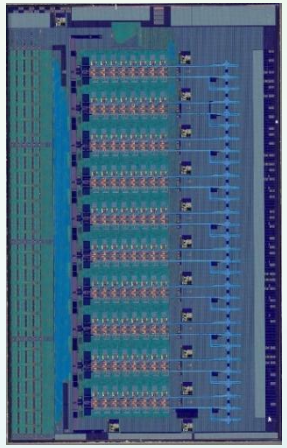
- Up to 1,000x smaller than optical devices in traditional ethernet transceivers
- High-speed capability
- Compatible with high volume 300mm CMOS[1]

Monolithic Integration



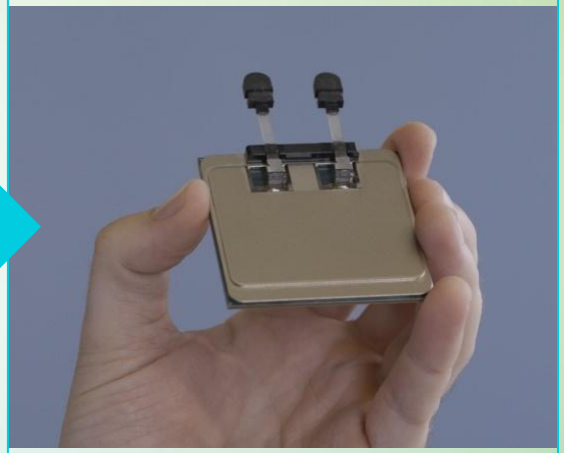
Dense integration of all electronics (TIAs, drivers, equalization, control) and photonics (waveguides, modulators, detectors) on a single CMOS chip

Optical I/O chiplets



- TeraPHY™ chiplet for in-package optical I/O
- Multi-Tbps with <5pJ/bit
- Nanosecond latency (no FEC required)

SoC In-Package Integration

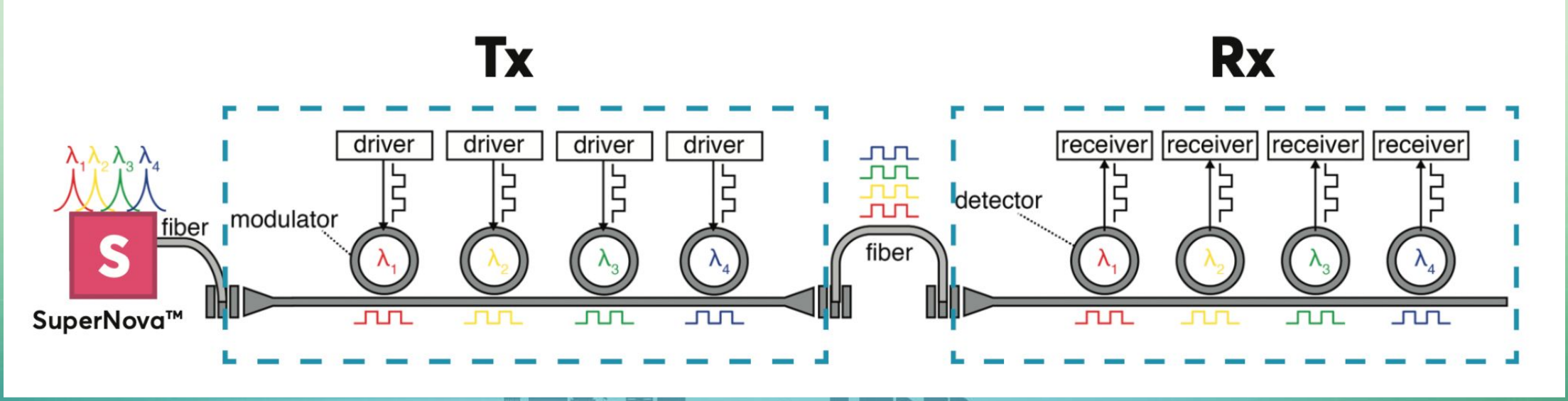


- Integration with state-of-the-art FPGA
- Direct from the package optical I/O

[1] https://gf.com/gf-press-release/globalfoundries-announces-next-generation-silicon-photonics-solutions-and/

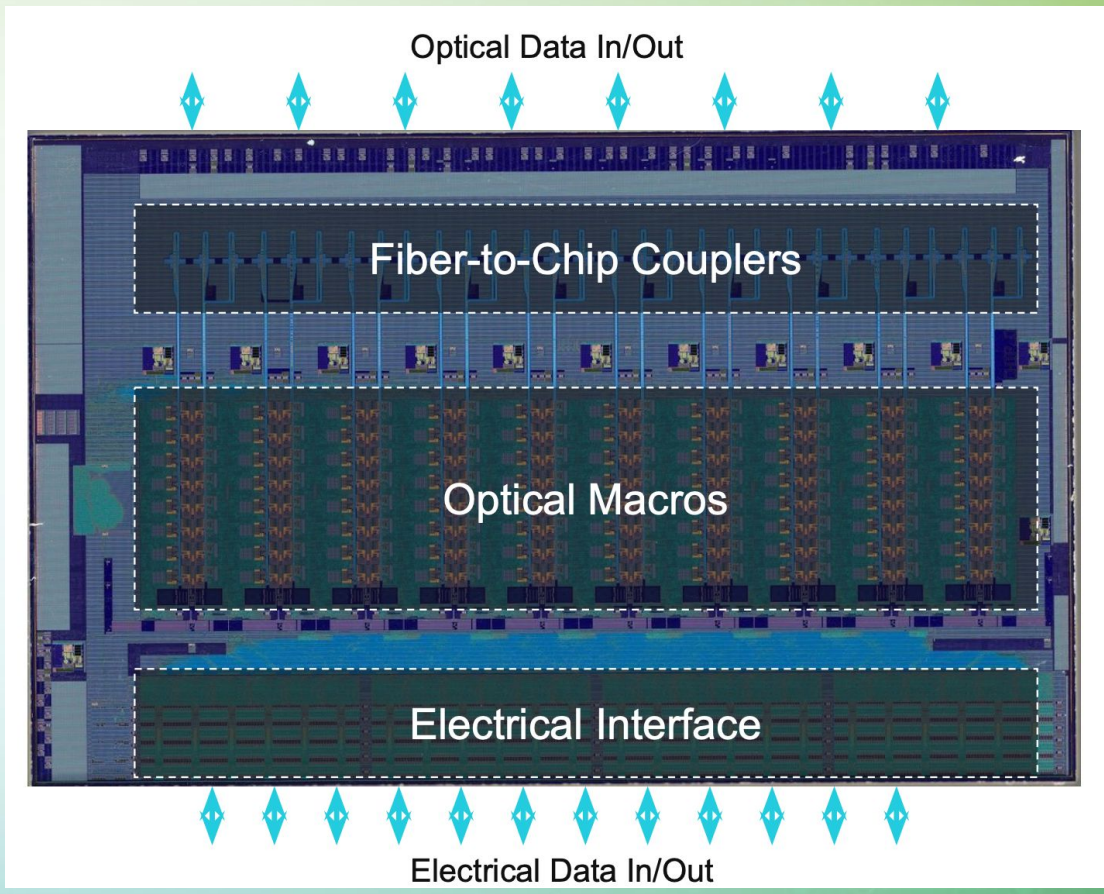
Technology

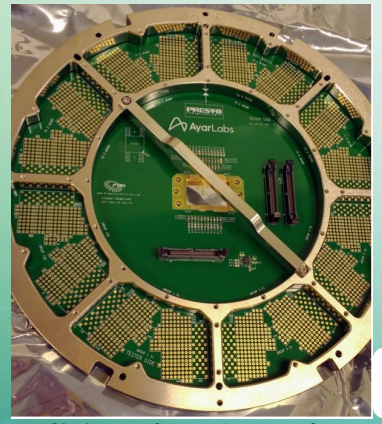
- Multi wavelength laser source for encoding data on multiple streams simultaneously
- Tunable microring modulators modulate transmission of specific laser wavelengths based on electrical data pattern input
- Microring resonators on receiver demuxes incoming data on specific wavelengths for conversion to electrical data pattern output



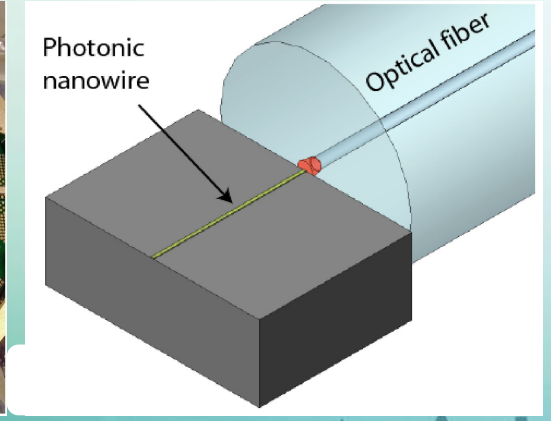
Technology

- **Reticle contains product and test chips**
  - Product chip
    - Horizontal edge couplers for optical connectivity
    - 1400 bumps for electrical connectivity
    - How do we screen for known good die?
      - Electrical wafer sort on standard 93k ATE





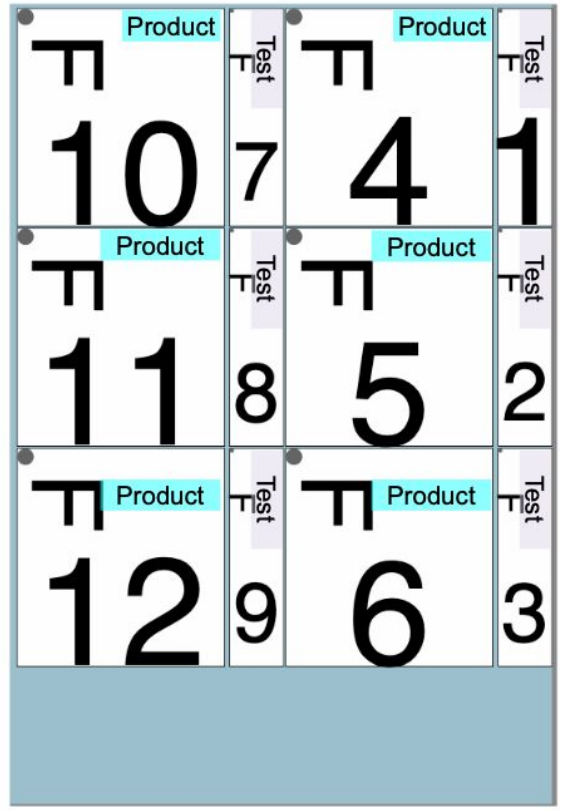
Traditional VLSI probe card -> no optical connectivity



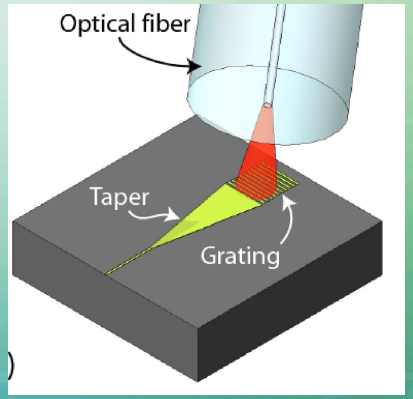
Horizontal edge coupler

Technology

- **Optical link is composed of multiple electronic + photonic components**
- **During NPI, we had test chips alongside product chips which contain independent device sites using vertical surface couplers**
  - Microring resonators (MRR)
    - Tx modulators (doped junction for electro-optic response)
    - Rx ring filters to select particular wavelength
  - Germanium photodetectors
  - Waveguides, NxN optical couplers, polarization splitter/rotators
  - Thermal phase shifters
- **Detailed high volume characterization of the components above is used to build a link model and estimate yield of product**



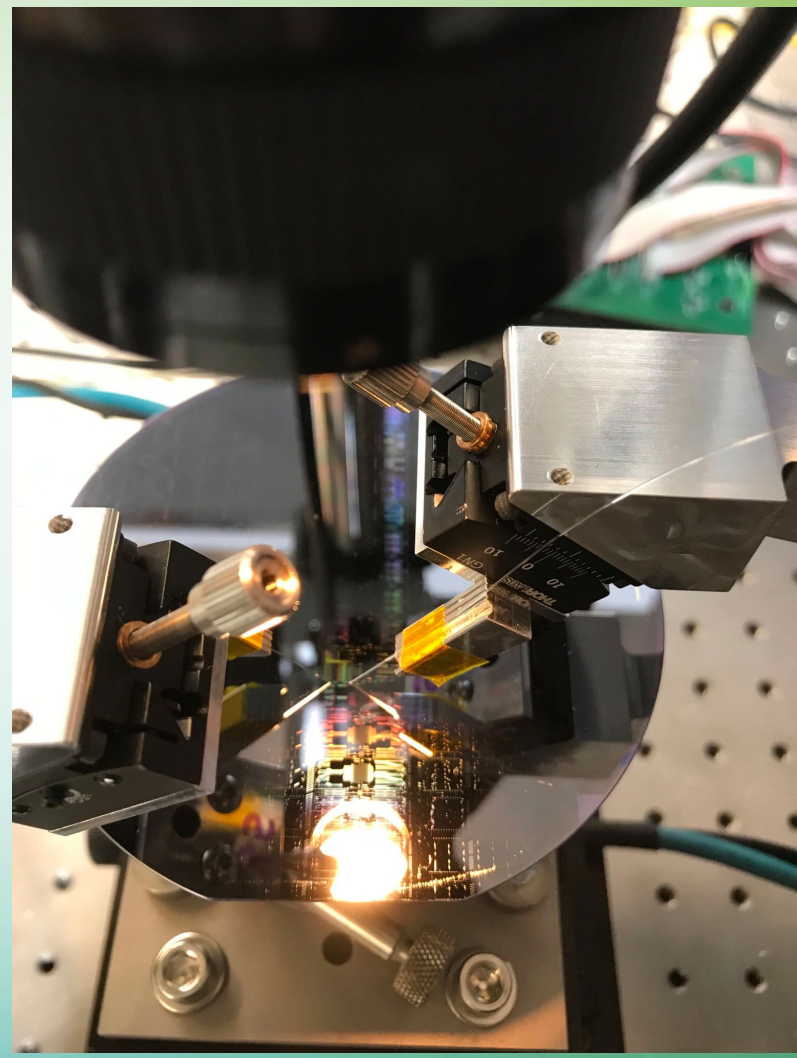
Reticle Plan



Vertical surface coupler

Early Characterization Setup

- **Manual test station**
  - Issues with repeatability and stability of two fiber setup (~0.5 dB)
  - Low throughput due to time it takes to align fibers after stepping them from site to site
  - Difficult to accurately set fiber height
  - No testing over temperature



CM300xi - SiPh Probe Station

- Enables automated full wafer optical + electrical characterization of various components that are used to build the TeraPHY™ chiplet
- Repeatable fiber alignment (~0.1 dB)
- Enables testing at high temperature (up to 150°C)

CM300xi - SiPh Probe Station

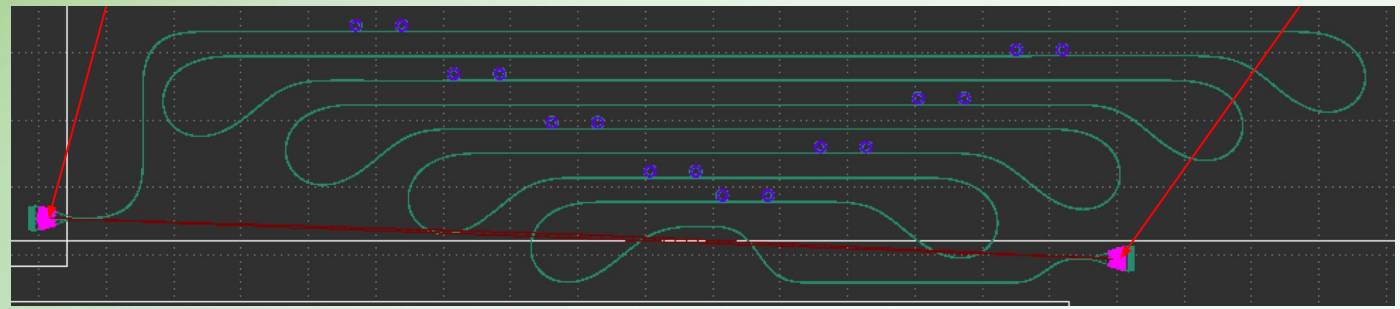
- Enables automated full wafer optical + electrical characterization of various components that are used to build the TeraPHY™ chiplet
  - Keysight swept laser system (Mueller matrix)
  - Optical switches
  - Polarization stabilizer
  - Variable optical attenuator
  - O-band amplifier Optical backscatter reflectometer
  - PCB to enable fiber alignment using photodetector current from DUT on wafer
  - Source measure units
  - Keysight PXI network analyzer (up to 53 GHz)
  - Thorlabs reference transmitter (up to 65 GHz)
  - Bit error rate tester and pattern generator remote head (up to 32 GBaud)
  - Keysight sampling oscilloscope

Examples of Test Sites

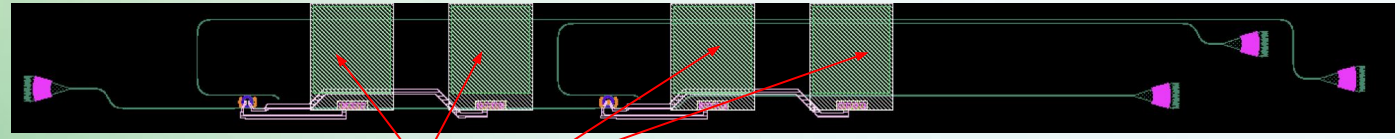
Input Grating Coupler

Passive

Output Grating Coupler

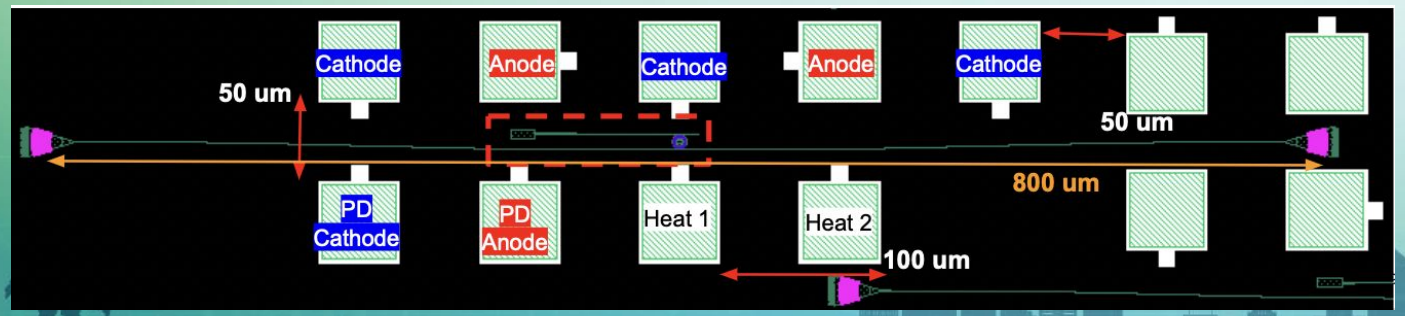


DC Electro Optic

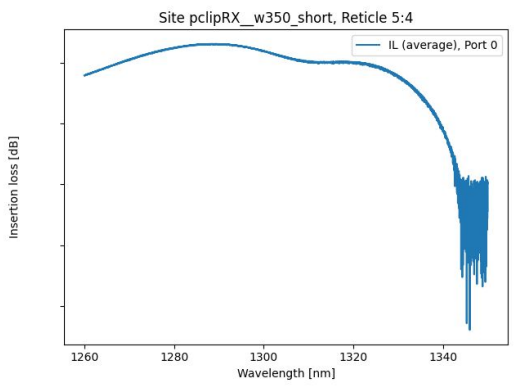


DC pads

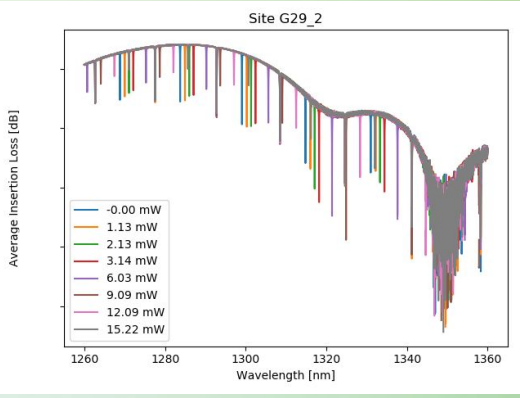
RF+DC Electro Optic (modulator)



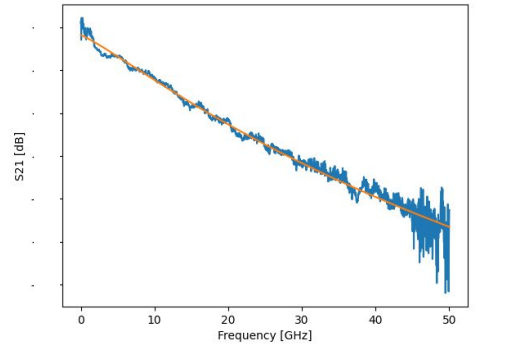
- Top pads are for RF characterization
- Bottom DC pads are for thermally tuning modulator resonance, and monitoring power inside the ring



Passive structure measurement



Thermal phase shifter



Photodetector S21

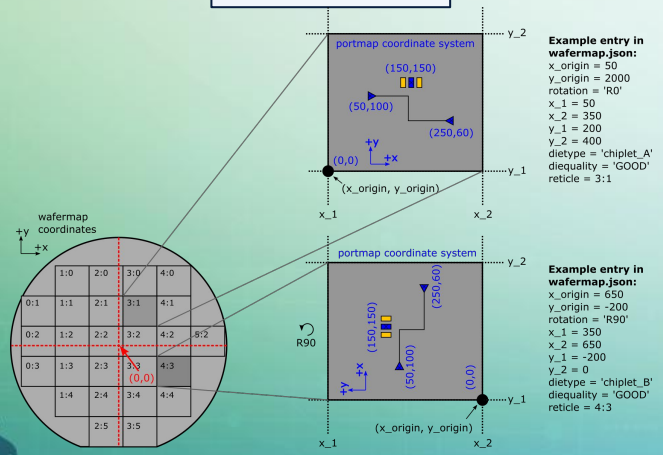
CM300xi-SiPh Test Executor

Wafer Map: Coordinates and dimensions of every subdie on wafer
Port Map: Coordinates of every optical port (grating coupler) and electrical port relative to subdie origin
Test Request: A table where each entry specifies a set of optical and/or electrical ports for a test site. It also specifies the measurement routine to execute and its parameters.

Port Map

```yaml
# port_map template
PD1_gc1:
  coordinates: [0.0, 0.0]
  directivity: 'WE'           # 'NS', 'EW', 'SN', or 'WE'. Convention: direction light travels from fiber-to-DUT
  type: 'optical'             # 'optical', 'electrical'
  chip_name: 'chiplet_Y'          # Chip name, as specified in the wafer_map
PD1_gc2:
  coordinates: [500.0, 100.0]
  directivity: 'EW'           # 'NS', 'EW', 'SN', or 'WE'.  Convention: direction light travels from fiber-to-DUT
  type: 'optical'             # 'optical', 'electrical'
  chip_name: 'chiplet_Y'          # Chip name, as specified in the wafer_map
PD2_gc1:
  coordinates: [0.0, 250.0]
  directivity: 'WE'           # 'NS', 'EW', 'SN', or 'WE'. Convention: direction light travels from fiber-to-DUT
  type: 'optical'             # 'optical', 'electrical'
  chip_name: 'chiplet_Y'          # Chip name, as specified in the wafer_map
PD2_gc2:
  coordinates: [500.0, 350.0]
  directivity: 'EW'           # 'NS', 'EW', 'SN', or 'WE'.  Convention: direction light travels from fiber-to-DUT
  type: 'optical'             # 'optical', 'electrical'
  chip_name: 'chiplet_Y'          # Chip name, as specified in the wafer_map
```

Wafer Map



Test Executor

Full Test Table

Each entry in full test table contains:
- optical and electrical ports in test site
- chuck coordinates
- hexapod coordinates
- measurement macro to execute
- measurement parameters

Test Request

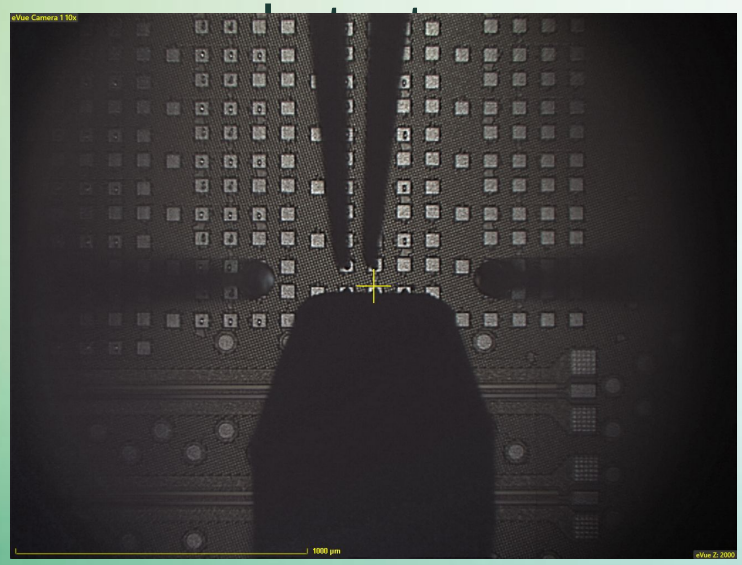
```yaml
test_table:
  - alignment_parameters:                  # Can override any defaults from Defaultalignment_parameters, such
      optical_input_port: 'PD1_gc1'             # Key for the corresponding port in "port_map"
      optical_output_port: 'PD1_gc2'            # Key for the corresponding port in "port_map"
      alignment_light_source: 'laser'      # Can be 'laser' or 'sled'.  This argument is optional.  Defaults t
      alignment_wavelength: 1290           # The wavelength used for laser alignment. If not specified, the wa
      electrical_port:                     # Key for the corresponding port in "port_map"
        south_pad_1: 'PD1_ground_1'
        south_pad_2: 'PD1_signal'
        south_pad_3: 'PD1_ground_2'
    measurement_macro:
      measurement_name: 'Insertion loss sweep'       # Label.  Doesn't affect measurement.
      macro_executable: 'il_pdl_sweep.py'  # Name of the python macro executable
      macro_recipe: 'il_pdl_sweep.yaml'    # YAML file with all parameters needed to run the measurement macro
    priority: 1
```

Improved Test Flow

- **Test throughput is still limited due to multiple factors**
  - Electrical probes need to be manually lowered/lifted. It is not possible to run electrical only or electro-optic tests, along with passive measurements.
  - Time taken to reconfigure and calibrate setup when switching between various types of measurements can be significant (1h ~ half day)
    - Ex. Two tier VNA calibration for RF measurements such as S11 (capacitance) or bandwidth (S21)
  - Test workflow
    - Set up hardware for passive test
      - Test wafer 1, wafer 2, …
    - Set up hardware for DC electrical only, and DC electro-optic test
      - Test wafer 1, wafer 2, …
    - Set up hardware for RF electrical only and RF electro-optic test
      - Test wafer 1, wafer 2, …

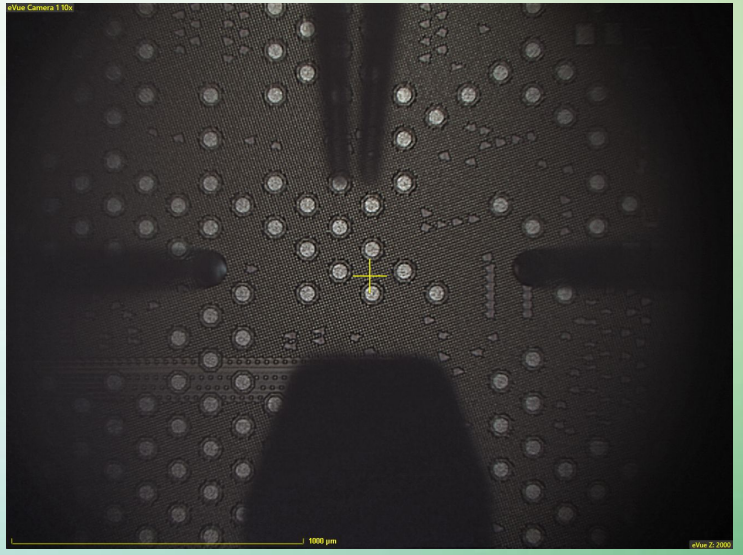
Improved Test Flow

- **Motorized positioners for allow us to achieve greater test integration**
  - Both RF and DC probes are loaded from south and north side respectively
  - Probe is lifted and retracted when not needed for a given measurement
  - RF calibration is monitored for drift, and periodically re-calibrated on ISS



Optical fibers, DC probe, and RF probe at home site

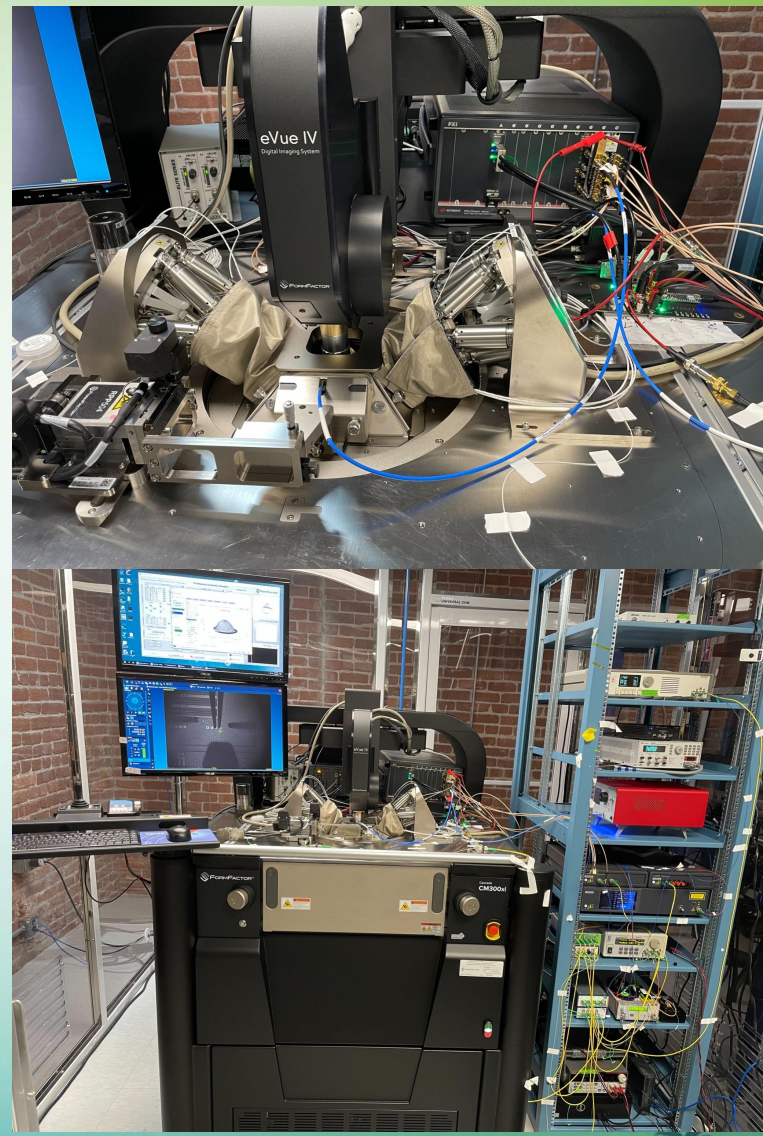
- Optical fibers and DC probe used for measurement
- RF probe lifted and retracted since it is unused



- Optical fibers used for measurement
- DC and RF probe lifted and retracted since they are unused

Summary

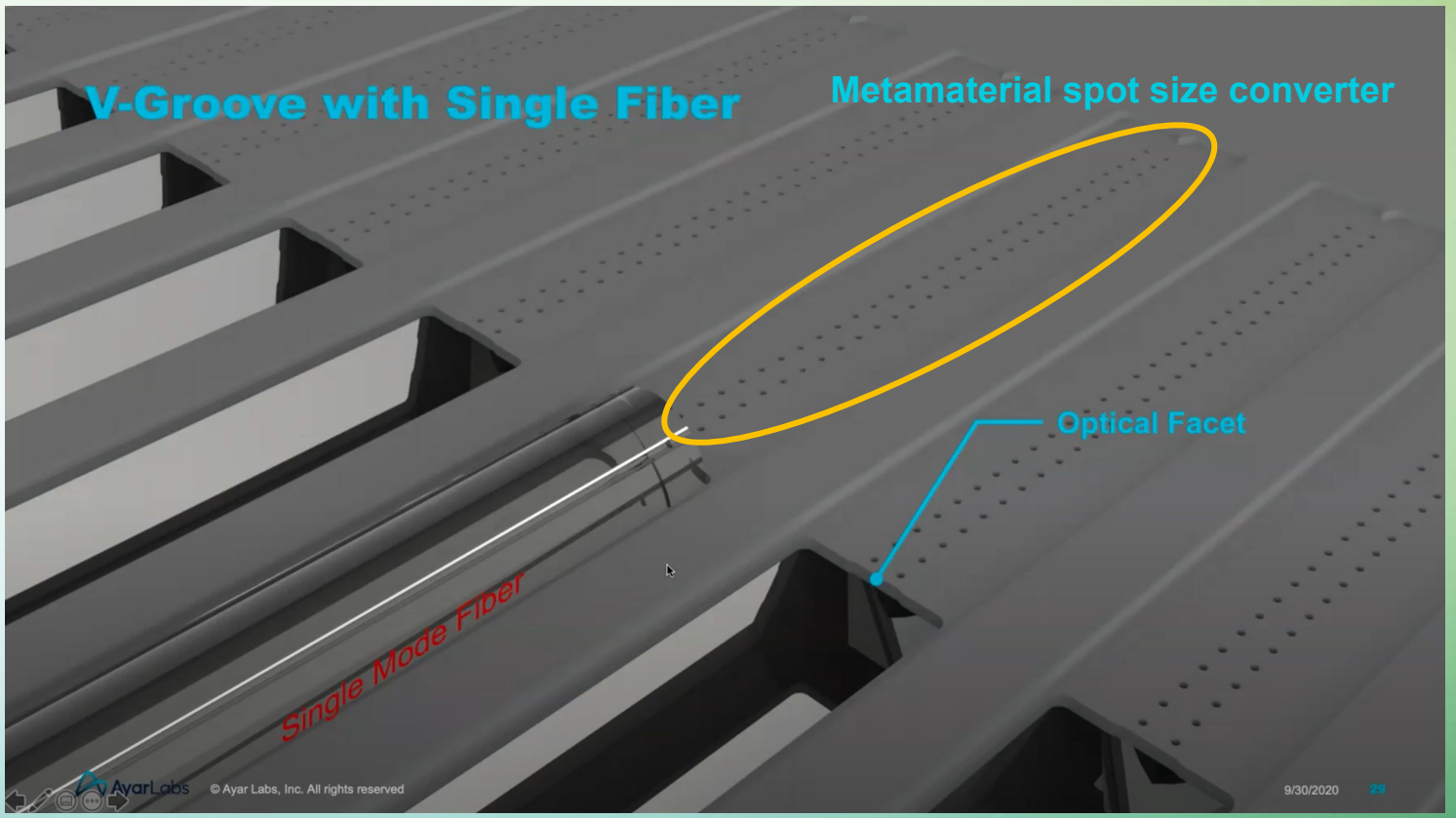
- **CM300xi-SiPh probe station enables us to characterize various electronic/photonic structures at scales needed to obtain statistical distributions with high confidence**
  - These parameters allow us to predict system performance
- **Motorized positioners allow for significantly increased test throughput**
  - Any combination of passive, DC, DC electro-optic, RF, and RF electro-optic measurements can be run over full wafer with no test setup re-configuration and calibration



Current Activities and Future Work

Ongoing Test Challenges

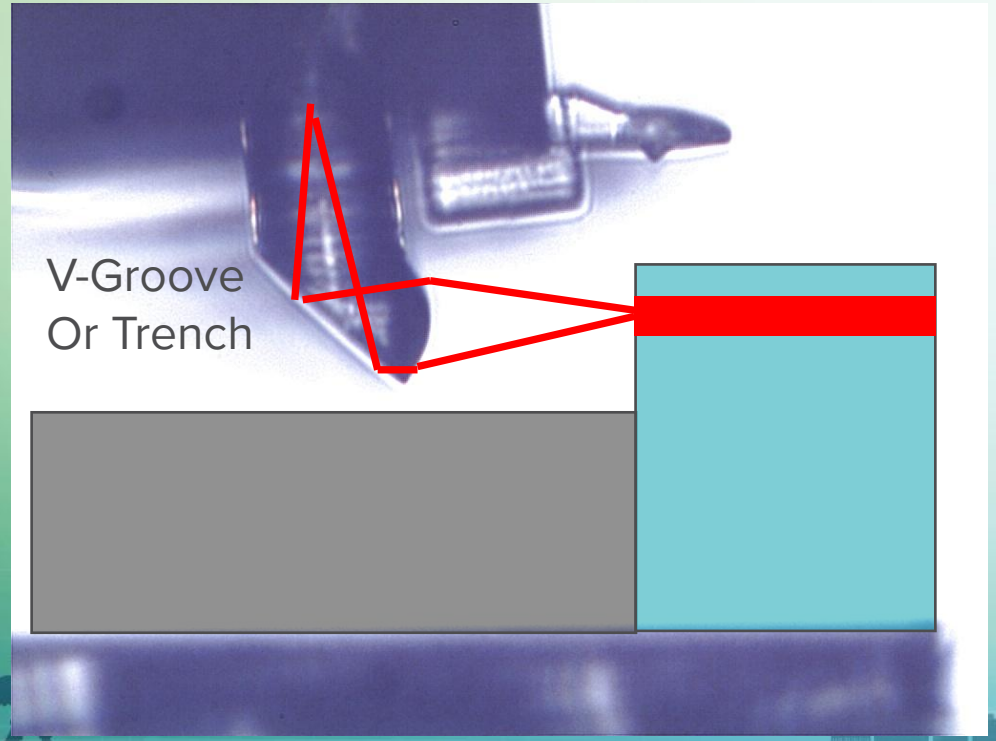
- **We want to have greater optical and electro-optical functional characterization of the actual TeraPHY™ product chiplet at the wafer level**
  - Requires probing at the wafer level through V-grooves for optical connectivity
  - Simultaneously need probe card that can land on all bump locations for electrical connectivity



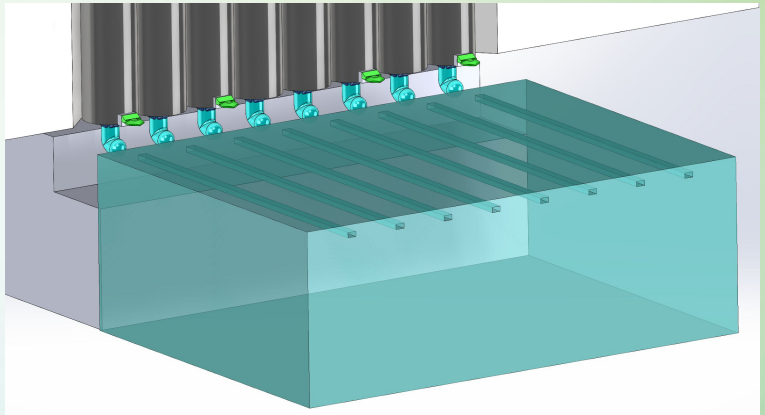
Current Work - Low Loss Wafer Level Edge Coupling

FormFactor™

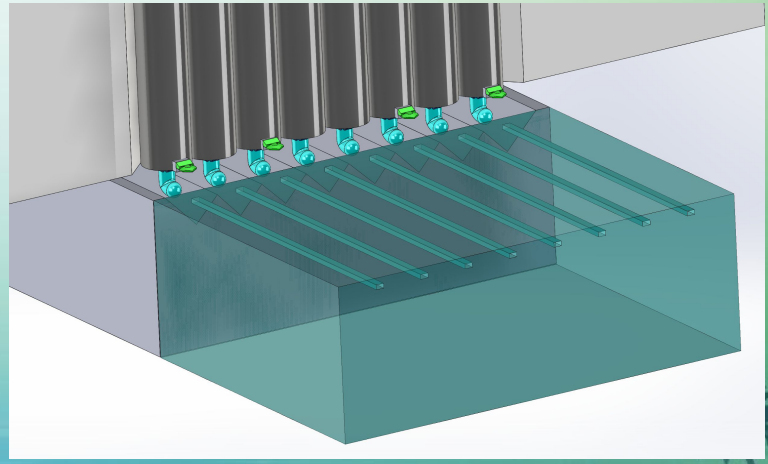
Pharos™ Technology



Wafer Level Trench



Wafer Level V-Groove

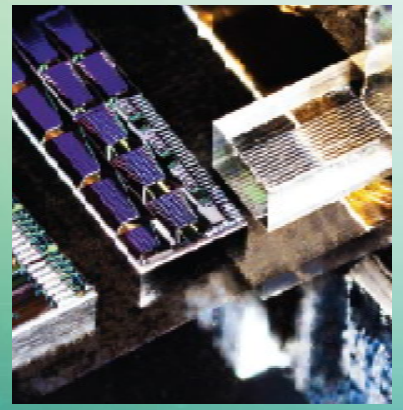


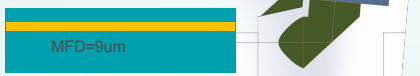
Pharos Low Loss Lens Performance for Edge Coupling

Singulated Chip: Chip1 MFD = 9 um
FF Pharos Lens: MFD = 6.0um
Structure: Loopbacks Edge Facet
Best coupling: WD=5um (Cleave fiber array) Power =-8.5 dBm
Coupling loss is 4.25 dB/facet
WD=38um (**Pharos Lens**) Power= 6.01-3.2 dBm
Coupling loss is **1.47dB/facet**

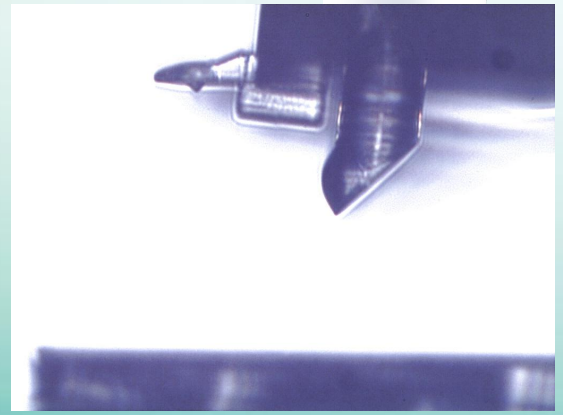
Cleave Fiber array

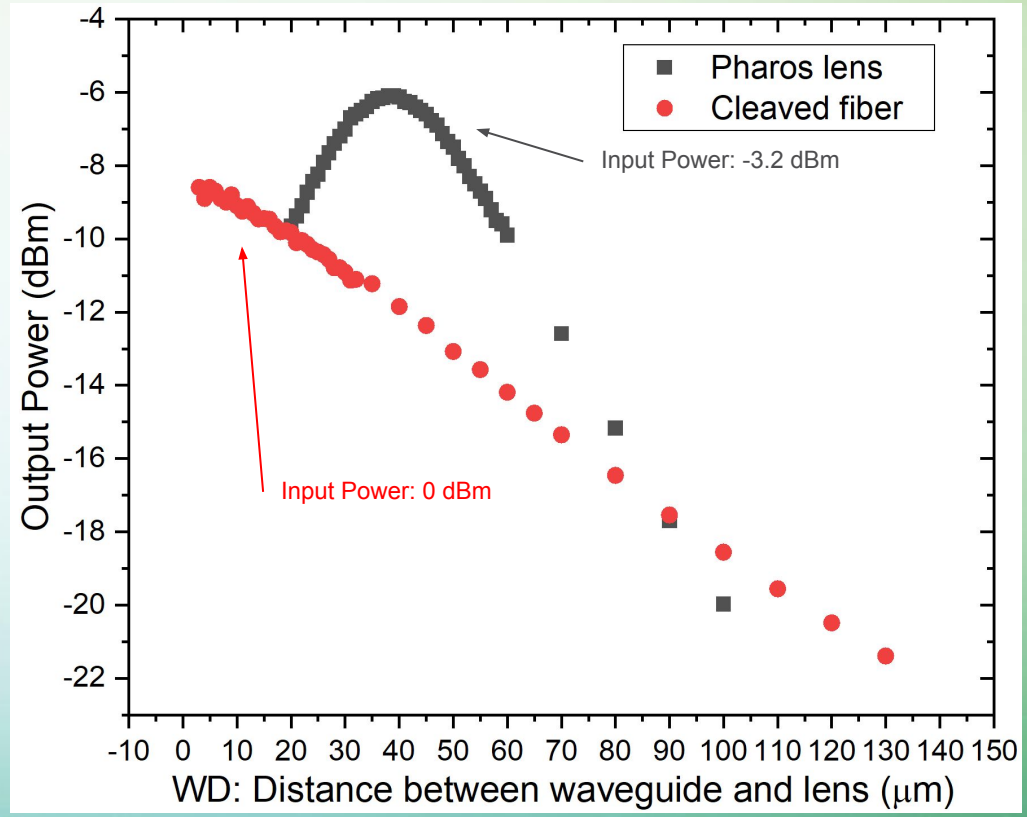
Red data





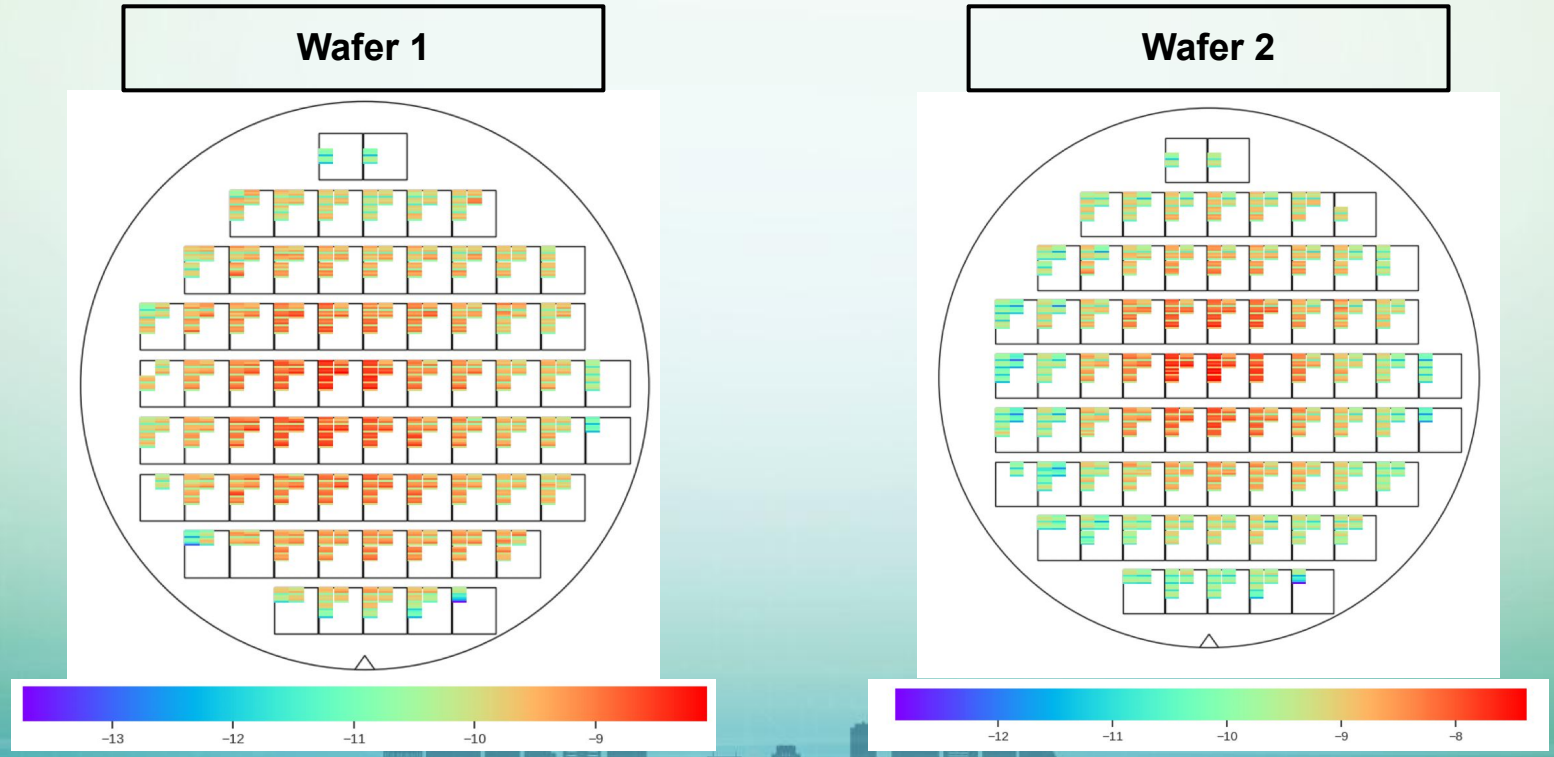
Black data



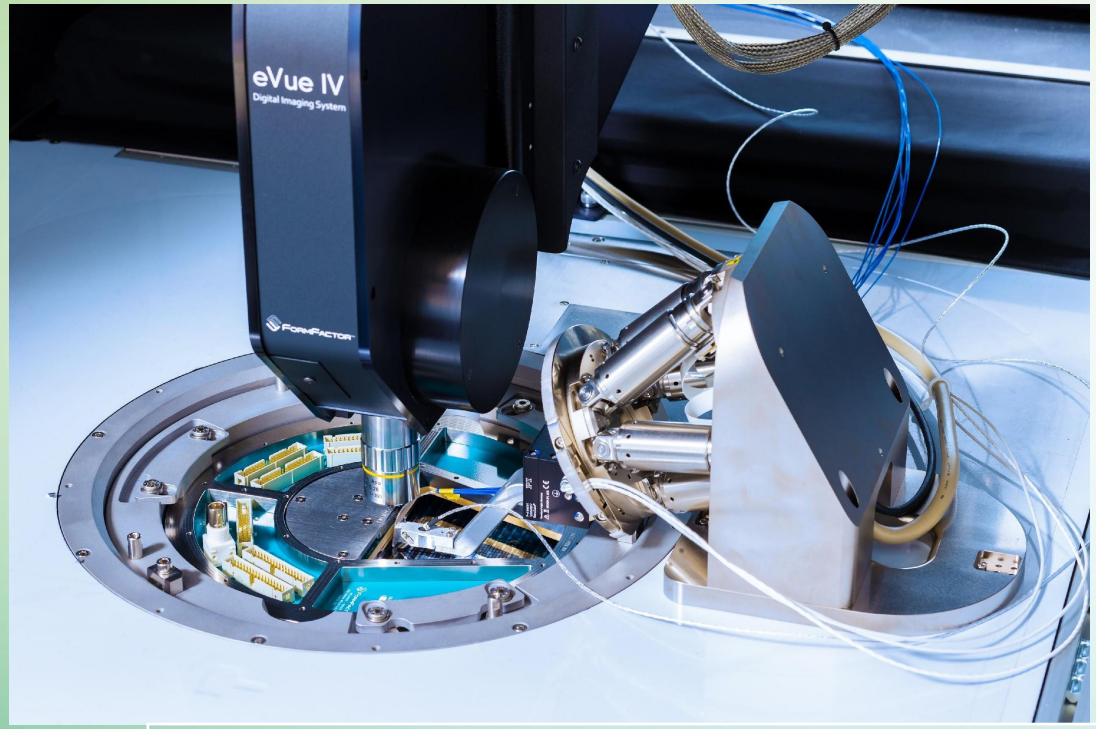


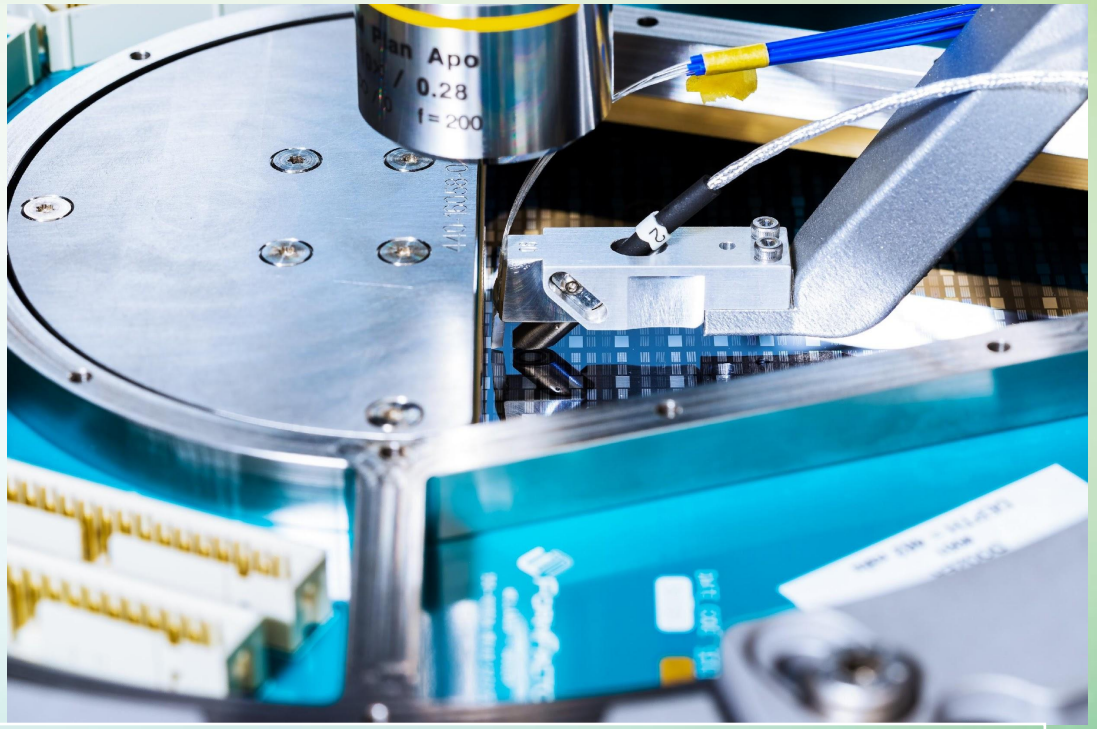
Application of FFI Pharos Technology

- Ayar Labs has performed full wafer measurements on dozens of wafers
- Insertion loss metric is being used as KGD screening criteria



Future Work – FFI Apollo Probe Card with Wafer Level Edge Coupling





Fully Automated Wafer Level Co-Packaged Optics Electrical-Optical Probing

Acknowledgements

- Forrest Sedgwick (Sr. Director of Test Engineering at Ayar Labs)
- Derek Kita (Sr. Staff Optical Design Engineer at Ayar Labs)
- Michael Rust (Sr. Staff Photonic Test Engineer at Ayar Labs)
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- Quan Yuan (Optical Design Engineer at FormFactor)
- Joe Frankel (Systems Engineer at FormFactor)
- Mike Simmons (Mechanical Design Engineer at FormFactor)