High Density Probe Card PCB’s,
Are you your own worst enemy to achieving Higher Parallelism on your Designs?

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June 2-5, 2019
Problem Statement

• As Probe Card PCB’s complexity increases, Most probe card designs have not paid enough attention to the Power/Channel Assignment.
  – An inefficient channel assignment can be the make or break issue to manufacturing your High Parallelism PCB
  – Good channel assignments give the best advantage to succeed
How do you know you have a problem?

• **Probe card vendors are asking you to change**
  – PCB Design is not routable
  – Can’t meet your parallelism
  – Layer count goes up, along with price
  – PDN reduced from target specification
  – Noise issues at test
  – Increased Lead time for Design
How bad can it really be?

- This Power/Signal routing was almost impossible. (<500 DUTS)
  - Increased Signal and Power layer requirements (over 200%) for both
This is what it could be!

- This is a real design in production today at 2007 DUT parallelism.
How do you fix your problem

• Do you review your own channel assignments?
  – If Yes,
    • You are helping your company achieve higher parallelism!
  – If No,
    • You may be your own worst enemy to achieving Higher Parallelism

• Creating a Tool for reviewing your assignments visually
  – Would be a great investment
  – Avoids waiting for Vendor feasibility analysis
  – Creates a more efficient Customer / Vendor hand off
Why is the Channel Assignment so Important?

• Complex designs are pushing the envelope of PCB manufacturing
  – We need to increase layers just to make the design possible!
  – Alternative manufacturing strategies may have to be employed
  – Even simple Designs will benefit from an efficient channel assignment

• Optimizing channel assignment decreases your complexity
  – A good assignment accounts for resource entry on the PCB
  – Reduces/Eliminates need for PCB Manufacturing/Routing feasibility
  – Increases layer density, and performance
• **Does the Tester limit an efficient assignment?**
  – Some testers restrict where assignments physically reside on tester
    • These may not be able to be resolved easily without talking to your Tester vendor
    • Example: Signal and Power resources placed physically separate on this interface

• **Is the Tester partially populated or has concentrated resources?**
  – Partially populated testers still produce a complex PCB,
    • Concentrated areas of routing and blank areas will require copper balancing
  – Increases your layer count
Solving Tester Limitations

- When testers have assignments that can’t be assigned radially,
  - The focus should be on the DUT array and not the tester

- This tester has resources concentrated in some areas of the tester

- By focusing the net assignments on the DUT array, a perfect channel assignment was still possible
  - Bottom image, routing was not possible

This is the same Design!
Solving Tester Limitations

• The pictures below shows all net classes separated to show how the signal assignment was optimized, despite the tester restriction

• This was a 4710 DUT Probe Card
  – Only 64 PCB layers
What makes a good Channel Assignment

• Radial Assignments in quadrants are always best
  – These make everything easy to route

Quadrants can be set either way, but crossing nets between quadrants creates conflict

No signals cross other groups from one connector
What makes a good Channel Assignment

- Avoid crossing Powers
  - Crossing powers is the #1 way to increase your layer count, and decrease your PDN performance
What makes a good Channel Assignment

- The Tester architecture will define where the longest traces go
  - Assigning longest nets at 45 degree angles creates longer overall routes
  - Sometimes 1 DUT will go to multiple sites on the board
What is my benefit when optimizing my own channel assignments?

• Improved Lead times for your Probe Card Delivery
• Eliminate routing feasibility work
• Lower Layer counts
• Shorter overall IO/DRV routing lengths (Improved Performance)
• Reduce likelihood of hitting PCB manufacturing restrictions
• Ability to reach the increased parallelism with fewer risks
• Simpler design at a lower cost
Thank you