SWTEST

PROBE TODAY, FOR TOMORROW

Hybrid MEMS Technology 2.0

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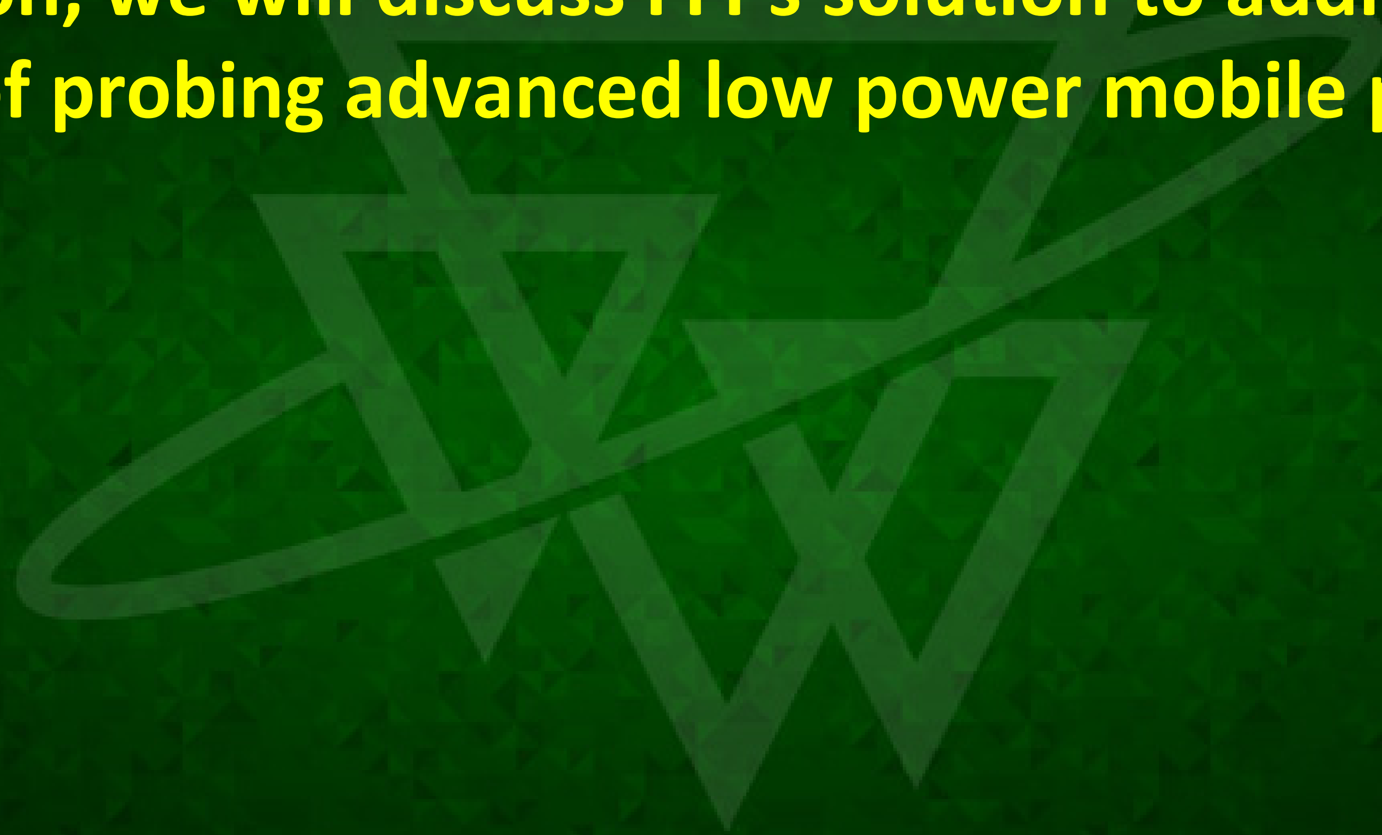
Agenda

- Overview
- Wafer Test Challenges
- Approach-Optimized Solution
- Results
- Summary

Overview

- **In this session, we will discuss FFI's solution to address the challenges of probing advanced low power mobile processors**



BACK IN MY DAY
ONE SIZE FIT ALL
imgflip.com

ONE SIZE FITS ALL?
FALSE.
ALL SIZES FIT ONE

Advances in Logic IC Process Technology Move Forward

Logic/Foundry Process Roadmaps (for Volume Production)

	2013	2014	2015	2016	2017	2018	2019
Intel	14nm finFET			14nm+	14nm++ 10nm		10nm+
GlobalFoundries	28nm		14nm finFET		22nm FDSOI	7nm 12nm	12nm FDSOI
Samsung	28nm 20nm	14nm finFET	28nm FDSOI	10nm		8nm	7nm EUV 18nm FDSOI
SMIC	28nm					14nm finFET	
TSMC	20nm	16nm+ finFET		10nm	7nm 12nm		7nm+ EUV
UMC	28nm			14nm finFET			

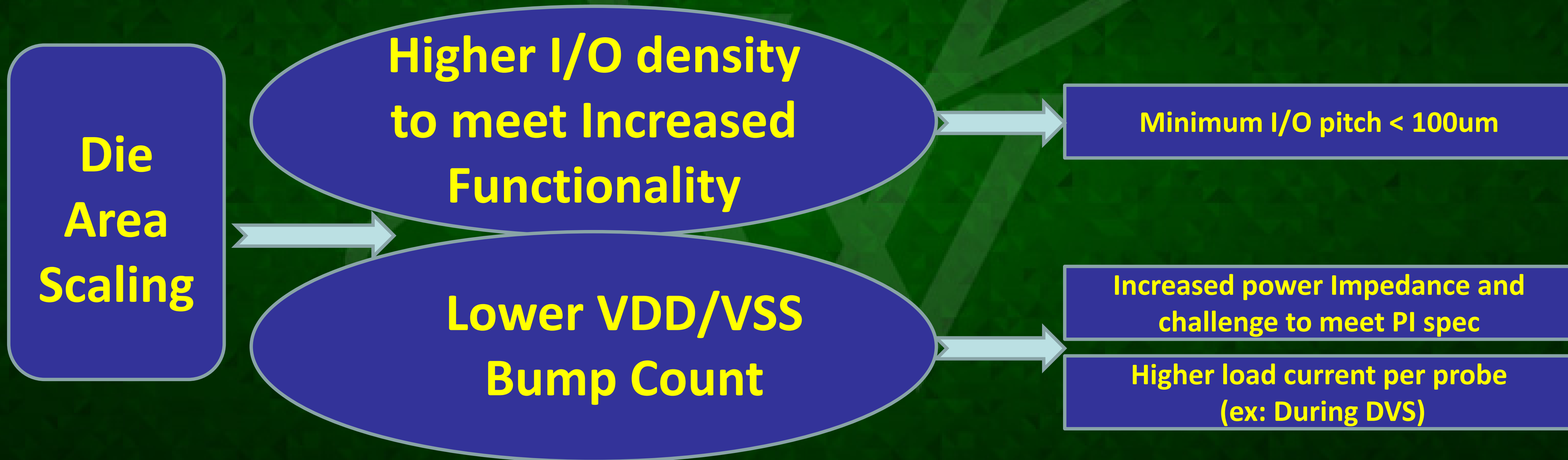
Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should be used only as very general guidelines.

Sources: Companies, conference reports, IC Insights

- Mobile and High Performance Computing (HPC) processors continue to lead the process node transition

Wafer Test Challenges

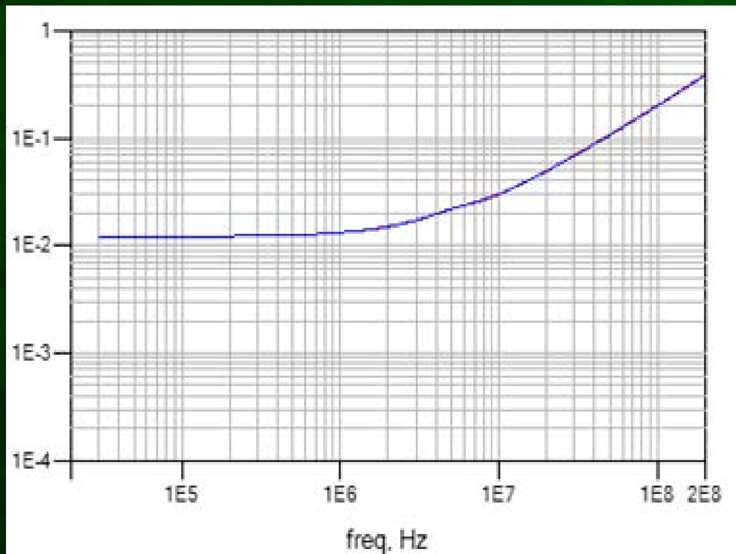
- Leading edge process nodes offer the benefits of smaller die size, higher performance and lower power consumption
- For wafer test, this means higher load currents, reduction in probe pitch and power impedance tolerance
- Challenge is to address these competing requirements with one probe design



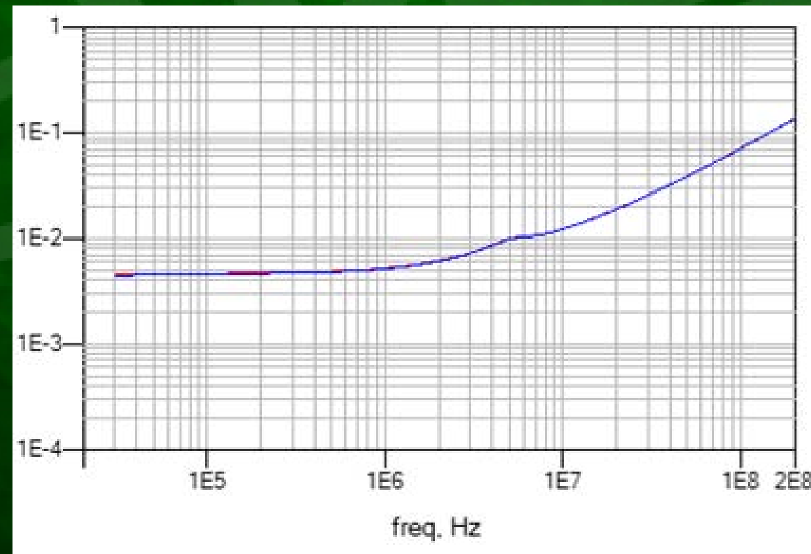
Lower VDD/VSS Bump Count Increases Power Impedance

- **Reduction in power bumps and adjacent ground bumps increases power impedance (PI)**
  - Due to increase in inductance and reduction in capacitance
- **More challenging for probe card design to meet customer PI requirement**

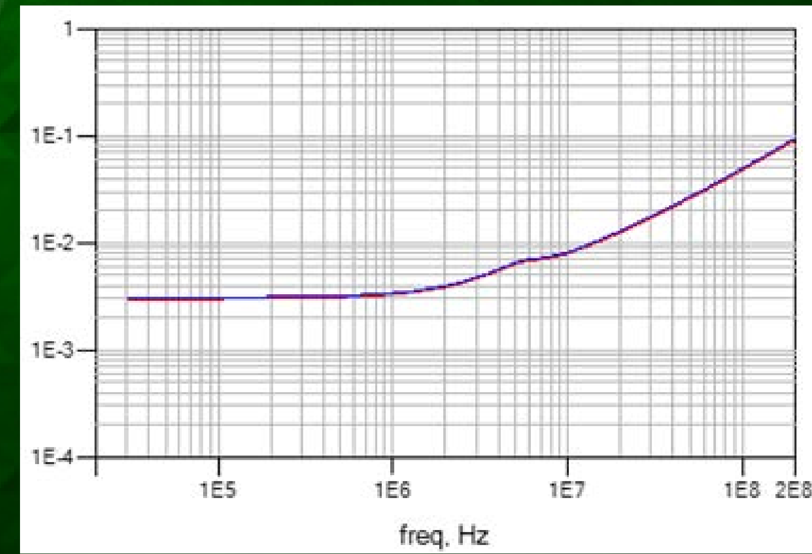
Number of Power Bumps: X



Number of Power Bumps: 2X



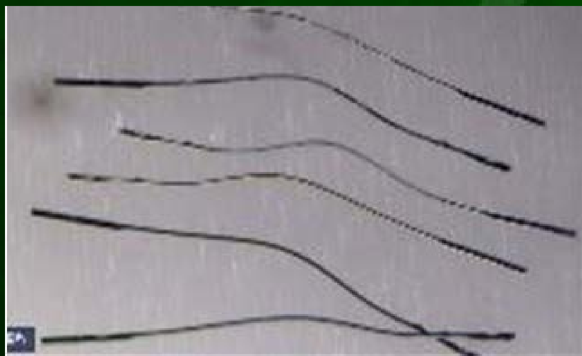
Number of Power Bumps: 4X



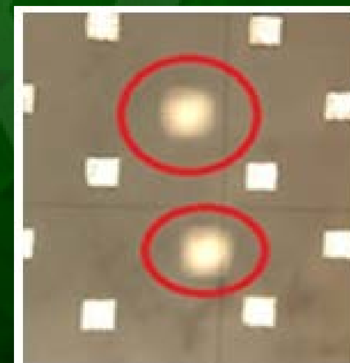
Dynamic Voltage Stress Test Needs Higher Probe MAC

- **Dynamic voltage test stresses a device at elevated voltage to eliminate early-life failures**
  - Typically at 1.4x to 1.7x device operating voltage
- **Devices that fail this test often generate large current surges through a subset of VDD/VSS probes before the initiation of power supply current clamps**
- **High MAC (Maximum Allowable Current) probe is desired to avoid burning probes and maximize uptime**

Deformed Probes due to current exceeding MAC

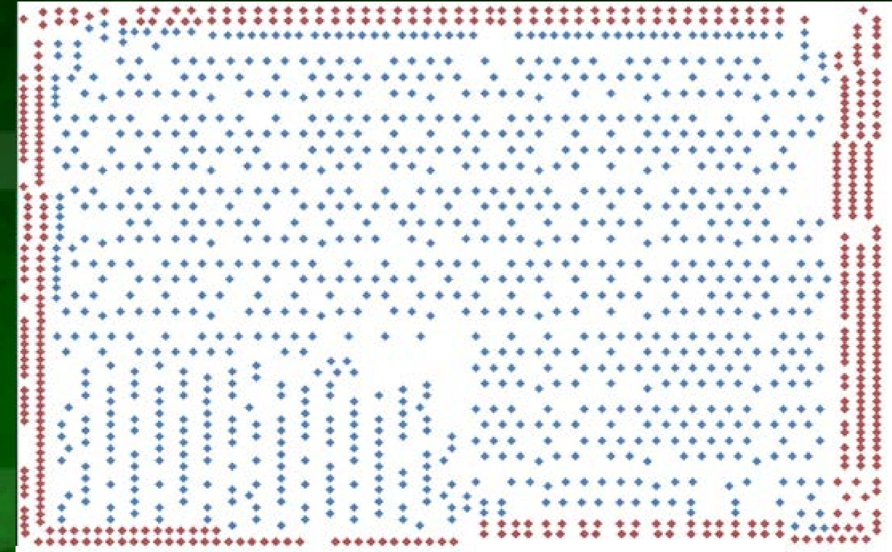


Deformed Probes exhibit planarity change



FFI Hybrid Solution: High MAC, Fine Pitch & Low PI in Single Probe Head

- Dual-probe design with composite (multi-material) probe structure
- Hybrid MEMS designs use different cross-section probes for different pitches
- Independent optimization of power, ground, and I/O probes
- Use finer pitch probe for IO's on perimeter of die and larger pitch probe for power/ground bumps in core area of die
- Satisfy multiple requirements, while "de-constraining" from a single-probe design

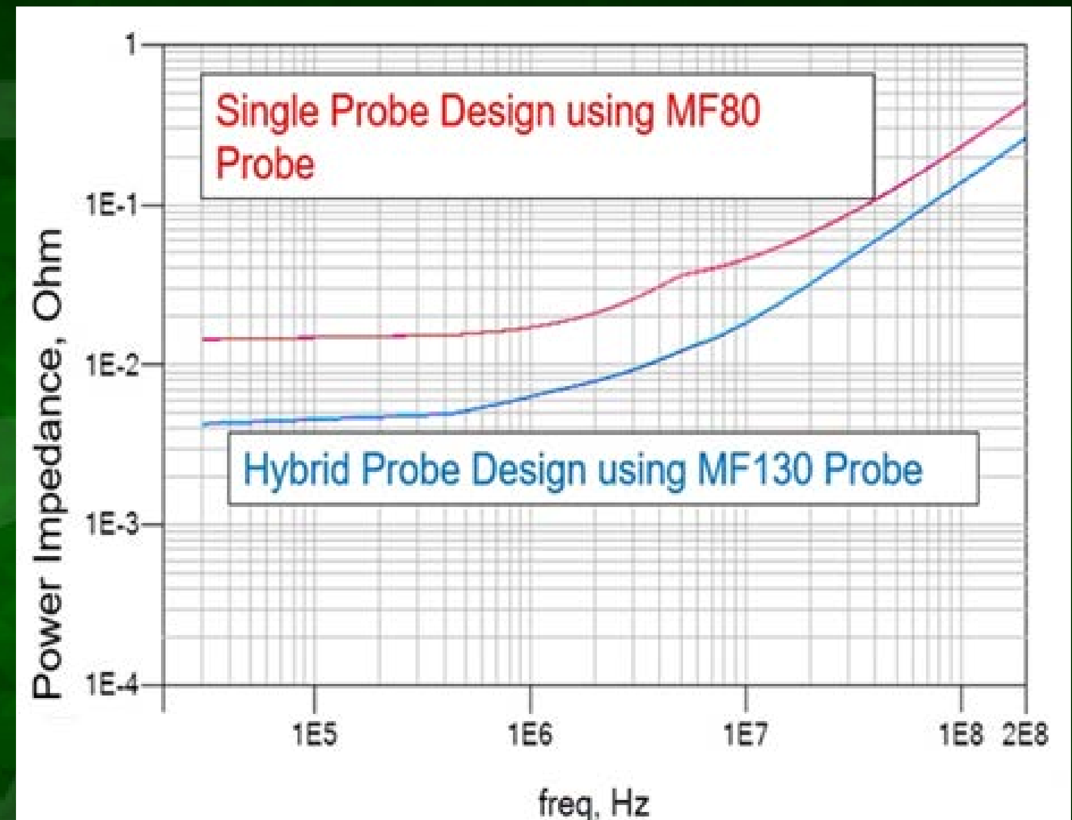


130um Pitch Probe
80um Pitch Probe

MF Hybrid (MF80F + MF130F) offers ~1.6X higher MAC for power probes Reduction in burnt power probes

Hybrid MEMS Probe Head Reduces Power Impedance

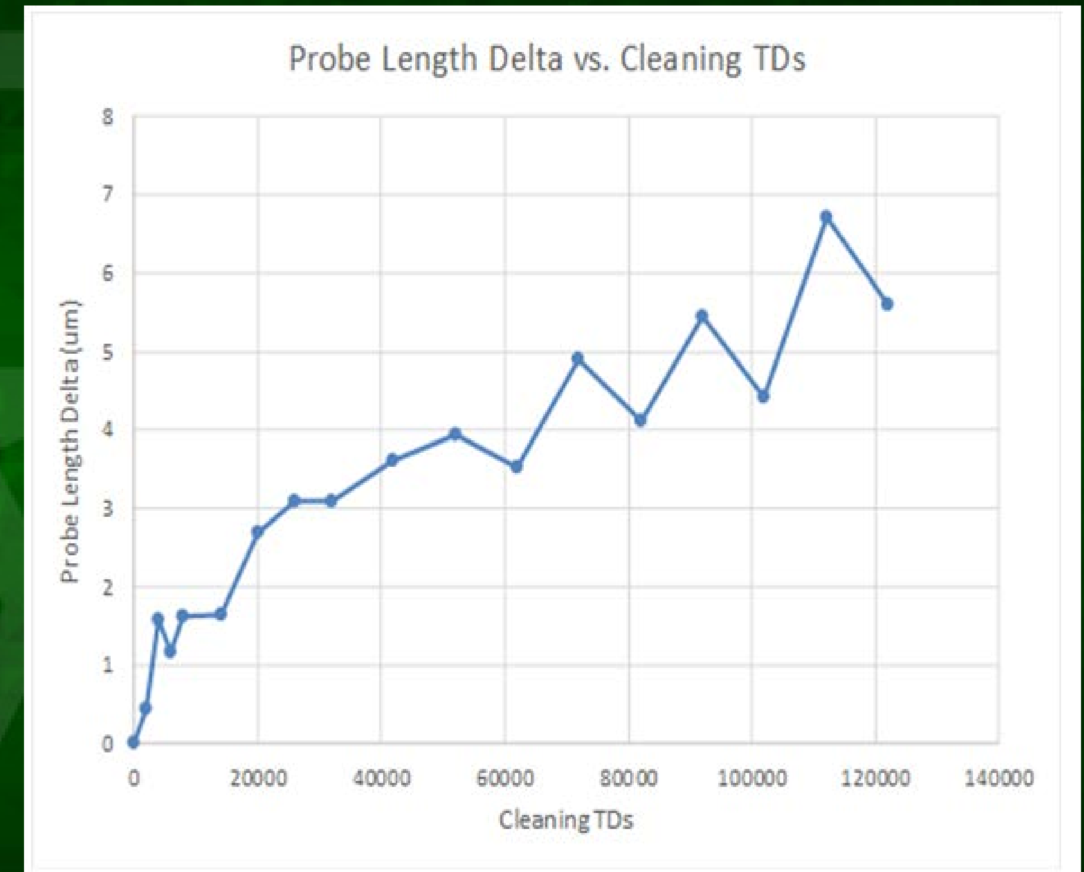
- PI comparison for critical Power supply with 17 bumps
- PWR & GND (MF130) probes enable
  - 40% lower Power Impedance



Note: Entire PC simulation that includes PCB, MLO and Probe Head

FormFactor Hybrid MEMS Tip Wear Rate Characterization (1/3)

- **Wear Rate Experiment Condition**
  - Progressive TDs completed on 3M Pink
  - 122k cleaning touchdowns
    - Equivalent of ~1M wafer sort touchdowns
  - 60um cleaning AOT Overtravel
    - Performed AOT/POT test to obtain the POT required to achieve desired AOT
  - Sample probes for each probe type at each corner of array were monitored for wear



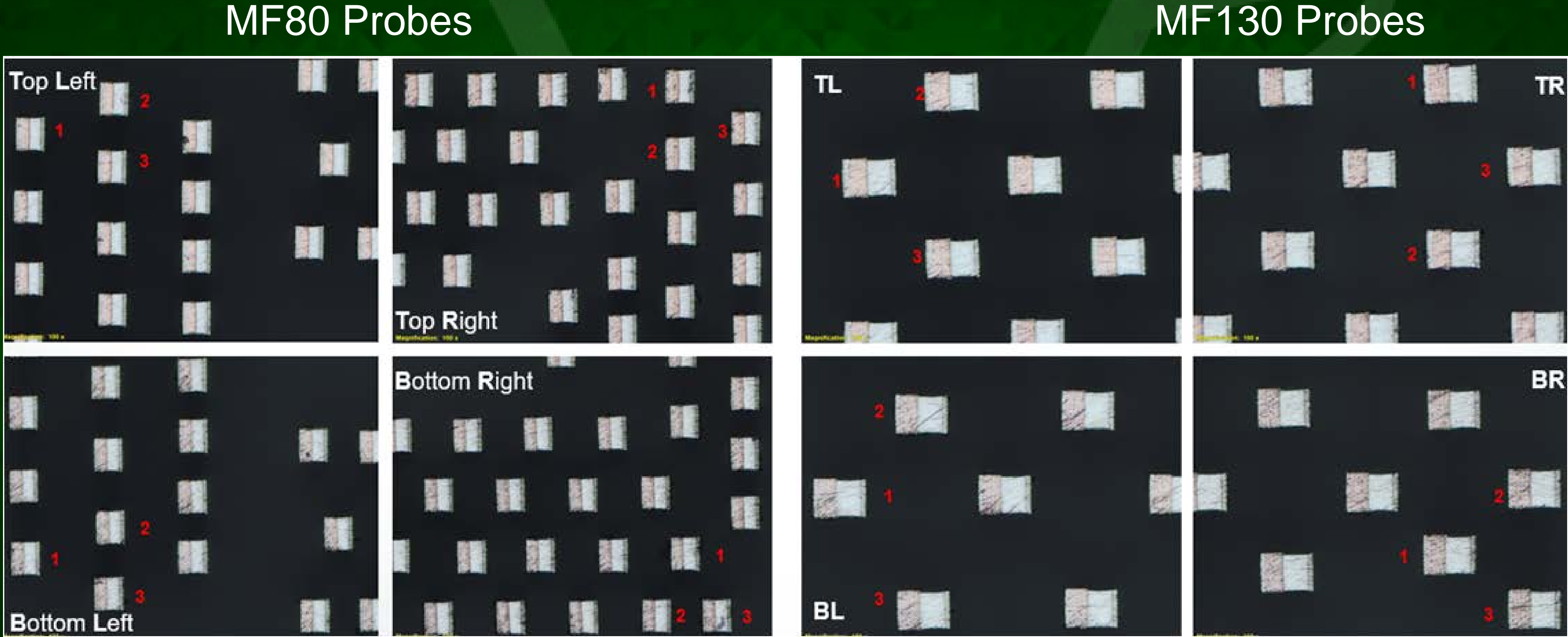
- **Experiment Results**
  - MF130F probes are ~6um longer than the MF80F probes after 1M wafer sort touchdowns
  - This 6um delta is well within acceptable tip length variation within a typical test cell

FormFactor Hybrid MEMS Tip Wear Rate Characterization (2/3)

- **Hybrid MEMS Probe Card Tip Wear Rate Experiment - Initial Probe Tip Pictures**

MF80 Probes

MF130 Probes

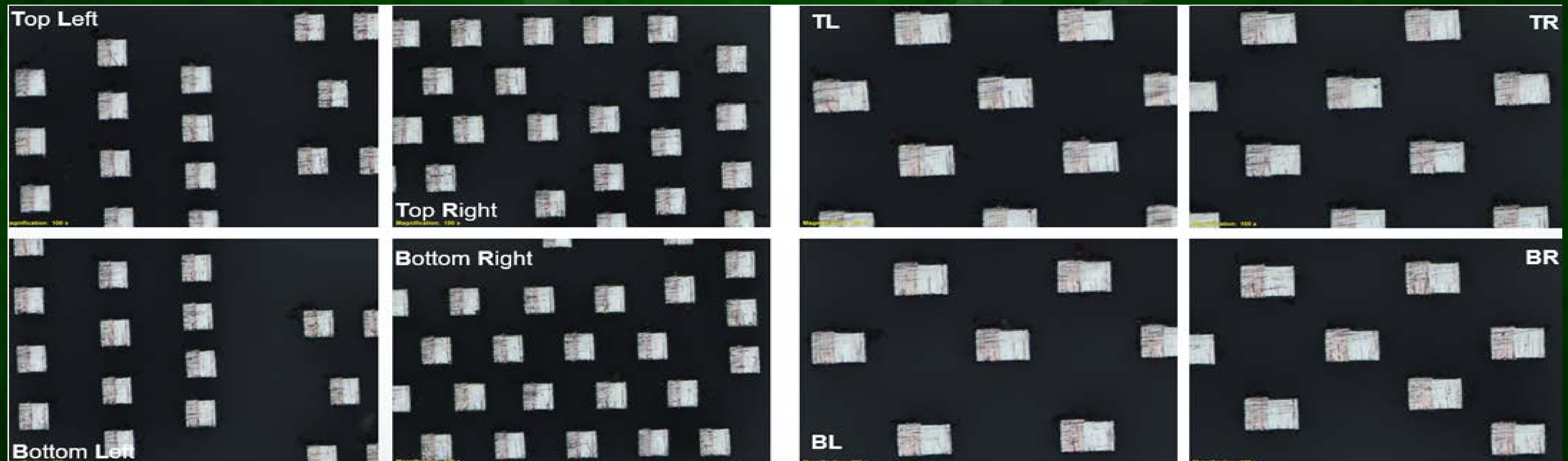


FormFactor Hybrid MEMS Tip Wear Rate Characterization (3/3)

- **Hybrid MEMS Probe Card Tip Wear Rate Experiment – Post Wear Probe Tip Pictures**

MF80 Probes

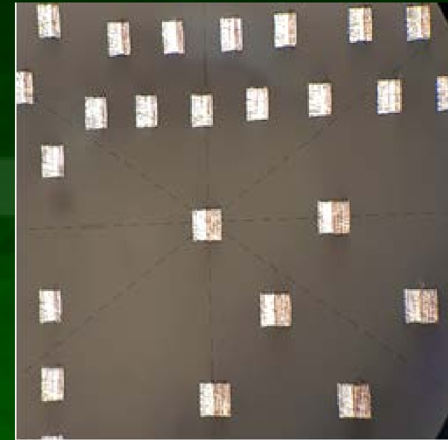
MF130 Probes



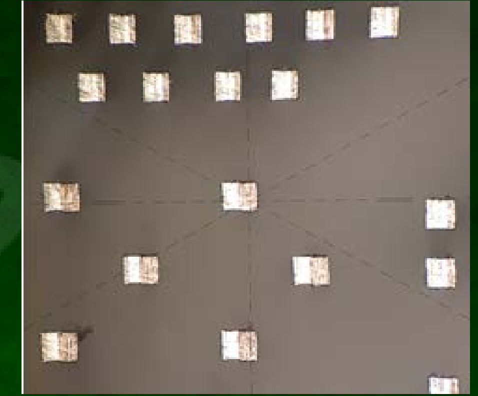
Customer Hybrid MEMS Results: Device X (1/2)

- **Design Parameters**
  - Total Probes: ~20,000
  - Hybrid Probe Types: ~70% MF100, ~30% MF80
  - Parallelism: 12 (2x6)
  - Bump Material: Cu Pillar
- **Results**
  - Yield and functional correlation passed with better results than single probe design
  - Expected even tip wear, no noticeable tip length difference after ~26K production touchdowns

Location	MF80-MF100 Delta
Upper Left	1-2
Lower Left	2
Upper Right	2
Lower Right	0
Middle	1

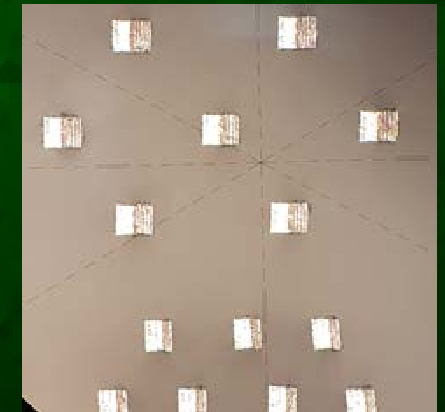


Upper Left



Upper Right

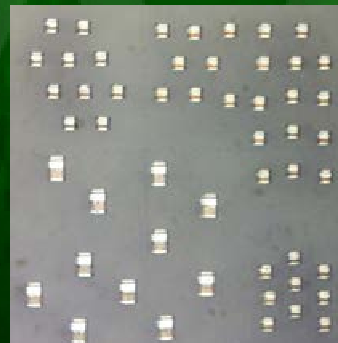
Lower Left

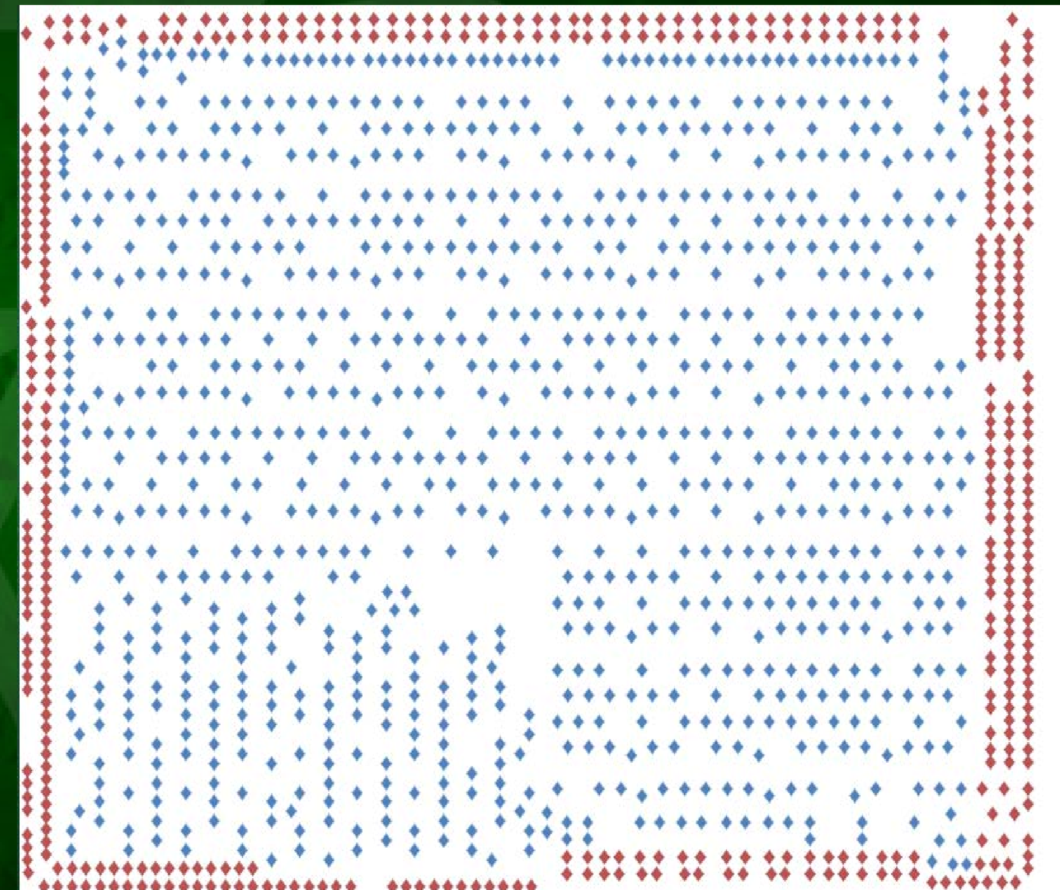


Lower Right

Customer Hybrid MEMS Results: Device X (2/2)

- **Design Parameters**
  - Probe Type: MF80 and MF130
  - Hybrid Probe Type: ~70% MF130, ~30% MF80
  - Total Probes: ~2000 probes
  - Bump Material: CuPillar
- **Results**
  - *No probe burn events for MF130F power probes*





FormFactor Hybrid MEMS – ALL SIZES FIT ONE

- **FormFactor Hybrid MEMS probe technology supports various competing requirements in a single probe head -- fine pitch, high current carrying capability, and lower power impedance**

- **Composite MEMS probe enables one principal probe design to achieve function/reliability at different pitches – simplify probe qualification process for customer**

- **Universal performance of hybrid probes has been demonstrated at customer production sites**
  - OT, Stress field, assembly, cleaning, maintenance, wear rate