Improving Signal Fidelity in High ParallelismProbe Card via TTRE

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Introduction

Focus of this discussion

• What this paper is “not”
  – SI/PI probe card design
  – FFI TRE
  – FFI ATRE and ATRE control method

• What this paper will discuss -
  – Using FFI Terminated TRE (TTRE) to achieve improved signal fidelity and enable higher signal sharing while maintaining or increasing test speed

TTRE is FFI patent protected
Outline

• Introduction of Terminated TRE (TTRE)
  – Signal line termination
  – DUT parallelism trend

• TTRE overcoming challenges of tester resource sharing
  – Signal degradation with higher TRE-share
  – Limitation on the number of signals shared

• Case study review

• Summary / Conclusion

• Follow-on work
Introduction

Increasing probe card parallelism with Advanced TRE

- Probe card DUT parallelism is trending higher enabled by higher signal sharing
- ATRE – Advanced tester resource enhancement/extension
  - DC and Power (PPS-TRE) with active components
- TRE / TTRE – DC signal share
  - TRE: signal and driver sharing without active components
  - Terminated TRE (TTRE): driver sharing with active components
- TTRE – recommended for TRE share of x14 or higher to improve signal performance and to increase test speed to 200MHz
- Address 1X, 1Y, 1Z process node transition

TTRE enables 200MHz with improved signal

TTRE is FFI patent protected
Introduction

What are TRE, ATRE, and TTRE?

- **Test Resource Enhancement = TRE**
  - Sharing of tester resources between multiple DUTs using passive components.

- **Advanced TRE**
  - Sharing of test resources using active components and having the ability to connect and disconnect DUTs from the tester resources
  - Other active circuits to increase tester capabilities
    - Current, Frequency ...

And the new TTRE = Terminated-TRE

TTRE technology improves signal condition which allows

1. Increased/doubled test speed without compromising signal integrity
2. Increased signal sharing without compromising test speed

TTRE is FFI patent protected
Signal Fidelity Impacted by Higher Sharing

- Key signal integrity considerations
  - Slow down rise time
  - Reduce signal amplitude
  - Increases signal skew

- Potential contribution to data-eye shrinkage

Example of signal impacted by sharing factor
Signal Fidelity Improves with Termination

- **Typical Issues with Signal Sharing/Splitting**
  - Voltage reflection at PCB to Share points
  - These cause driver signal arbitrations that limit performance
    - Amplitude, rise time, etc.

- **TTRE absorbed the reflections, enhanced the signal**
  - Minimized signal reflections from V-share back to driver
  - Absorb reflection from VDUT back to V-share and source
  - Significant improvement in waveform at the DUT
    - Increase amplitude, restore rise time

**Characteristic Impedance fundamentals**

\[
Z_0(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left[ \frac{5.98H}{(0.8W + T)} \right]
\]
Key Benefits of TTRE Implementation

- Enables higher parallelism (>1536DUT) while maintaining test speed at ≤125MHz
  - Without TTRE higher signal sharing reduces signal fidelity
    - Slower rise time, reduction of amplitude
- Maintaining parallelism (1536DUT or 2112DUT) while increasing test speed from 100MHz to 200MHz
  - Better signal fidelity at higher test frequency
- Improve throughput and test efficiency
  - Test coverage increases with test frequency increases
- Extend life time and ROI on existing tester fleet
- Package device to wafer sort test result correlation at elevated 200MHz
TTRE Implementation Considerations

There are different ways to implement TTRE depending on tester capability

– Termination values (RT and VTT) selected according to signal performance, power dissipation, and tester driver capability
  • (i.e. 28ohm, 45ohm, or 57ohm based on # of share)
– Internal switch available to isolate TTRE during DC and low speed testing
– TTRE power supply provided on probe card
  • Programmable from ATE voltage resource (e.g. unused driver, DC channel or PPS)
Typical Tester Channel with TTRE Implementation

- **Address / command clocks and differential inputs**: 
  - CS_A
  - DQ_A
  - CK_T_A
  - CK_C_A
  - DQS_T_A
  - DQS_C_A
  - CA & WCK (for DDR5/LPDDR5)

- **Typical test items improve with higher test frequency**: 
  - Easy functional
  - Complex functional
Case Study: >10-TRE Share Analysis

- **Simulation conditions**
  - Frequency = 100MHz, 175MHz and 200MHz
  - Vin = 1.1V, VTT = Vin/2
  - Magnum5 Tester
  - 1.0pF Load

- ATE driver input
- Probe Card
- VNA Measured
- S-parameter
- DUT
- 1pF cap load

- Data eye evaluation point

- Keysight ADS
- Cadence Sigrity
>10-TRE Share, 1.1V, 100MHz, 175MHz, 200MHz

- TTRE greatly improves signal amplitude and overall data-eye opening

**Table:**

<table>
<thead>
<tr>
<th></th>
<th>FFI</th>
<th>TTRE</th>
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<tbody>
<tr>
<td><strong>100MHz</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>175MHz</strong></td>
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<td></td>
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<tr>
<td><strong>200MHz</strong></td>
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**With TTRE**

- Enables higher ATE signal resource sharing while maintaining test quality
- Enables higher probe card parallelism for 1TD i.e. 2000 to 3000DUT
- Enables double speed from 100MHz to 200MHz without compromising test quality
- Enables early time to PGK test result at 200MHz
## Case Study Review

### X16-TRE Design with TTRE for LPDDR4

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ML9431A</th>
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<tbody>
<tr>
<td>Device</td>
<td>LPDDR4</td>
</tr>
<tr>
<td>Tester</td>
<td>MGV 24 Site</td>
</tr>
<tr>
<td># of TTRE Module</td>
<td>~200</td>
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</table>
| Max Parallelism Supported | 1536  
                          | 2048 (16SA)   |
| Probe count             | >100K         |
| Touchdown               | 1TD           |
| Total net count         | ~25K          |
| Total switch count      |               |
| DC & PPS TRE IC         | ~200 XDC Boost |
Actual Wafer Test Measurement

- Overall efficiency achieved depends on the number of frequency related test items implemented and test strategy
- Proven test frequency doubled from 100Mhz to 200Mhz in production environment for DDR4/LPDDR4 type memory (1X and 1Y node)
  - Correlated between wafer test and final package test result
  - No deviation from fail bit count
ATE Test Program Considerations

- **Test Program considerations for TTRE Implementation**
  - PPS channel assignment of dummy DUT to set up the reference level.
  - Tester spec consideration for TTRE power consumption.
  - Control bit assignment for TTRE On/Off.
  - VIH/VIL level adjustment by each test items.

  --> Consider levels based on VIH / VIL variables

<table>
<thead>
<tr>
<th>VTT = 0.75V setting @ 1.5V Operation</th>
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<tbody>
<tr>
<td>ATE VIH</td>
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<tr>
<td>DUT VIH</td>
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<tr>
<td>ATE VIL</td>
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<tr>
<td>DUT VIL</td>
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</table>
Device Specific Test Correlation

- Device specifics test results
  - Performance improvement in term of test speed
    ① Successfully achieved test speed increased from 100Mhz to 200Mhz
    ② Function test time reduction
  - Strong 100Mhz Vs. 200Mhz wafer test correlation results
    ① No deviation from wafer fail bit count
  - Strong Wafer test Vs. PKG test correlation results
    ① No deviation from fail rate & yield
Summary / Conclusion

• Terminated TRE (TTRE) significantly improves signal fidelity, enables higher tester resource sharing as DRAM node transitions to 1X, 1Y, and 1Z on existing testers
  – Higher test frequency with wider and larger data-eye
  – Higher probe card DUT parallelism

• By doubling test frequency from 100MHz to 200MHz, TTRE improves test throughput and efficiency
  – Faster clock, more efficient functional tests

• Enable correlation and early time to data for packaged test result at 200MHz
  – No deviation from wafer test & package test result at elevated test speed of 200MHz
Follow-on Work

- Implementing and validating TTRE at TRE-share >x30 to enable 1TD testing of ~2500 and ~3000DPW using existing ATE
  - Enabling testing of DRAM 1Z process node transition
  - 1TD, 200K probes per probe card, ~3000DUT parallelism
- Data-eye opening performance improvement with FFI TTRE technology

- No TTRE
- >x30-TRE Share
- 125Mhz

- With FFI TTRE
- >x30-TRE Share
- 125Mhz
Thank You - Questions

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