



SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

Next Generation DRAM Temperature Requirements and Impacts to Full Wafer Contactor Probe Card Performance

SAMSUNG



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True? or False?

**We don't barbecue the cellphone
and laptop.**



Overview

- Automotive IC Market Overview
- Automotive IC Test Requirements and Probecard Challenges
- FormFactor High Temperature Probecard Solution
- DRAM wafer level reliability test requirements and Grade-0 test result
- Summary and Acknowledgement

Automotive IC Market Overview

- **Key Drivers**

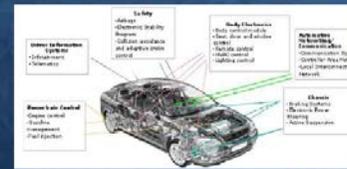
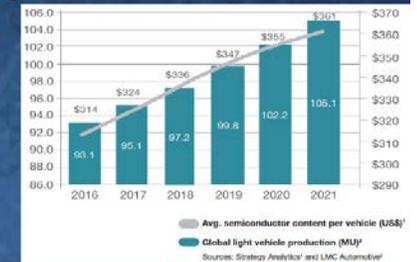
- Critical Safety System
- Increased fuel efficiency
- Navigation and communication
- Comfort & Entertainment features

Automotive Semiconductor Market Overview

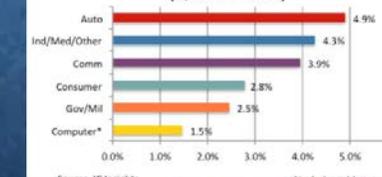
Drive Demand of New Testing Solution

- **Automotive electronics is a fast-growing market**

- Predictions are between 3%~12% CAGR over next 5 years
- Average number of semiconductors in a car increases significantly in modern cars
- Key drivers for automotive IC growth
 - Critical safety system
 - Increased fuel efficiency
 - Navigation and communication
 - Comfort & entertainment features



Worldwide Electronic System CAGRs (\$, 2015-2020)

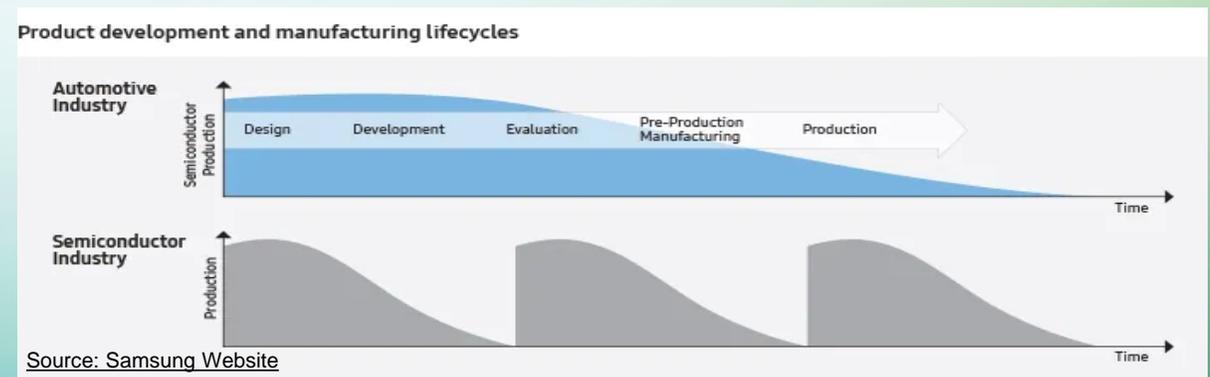
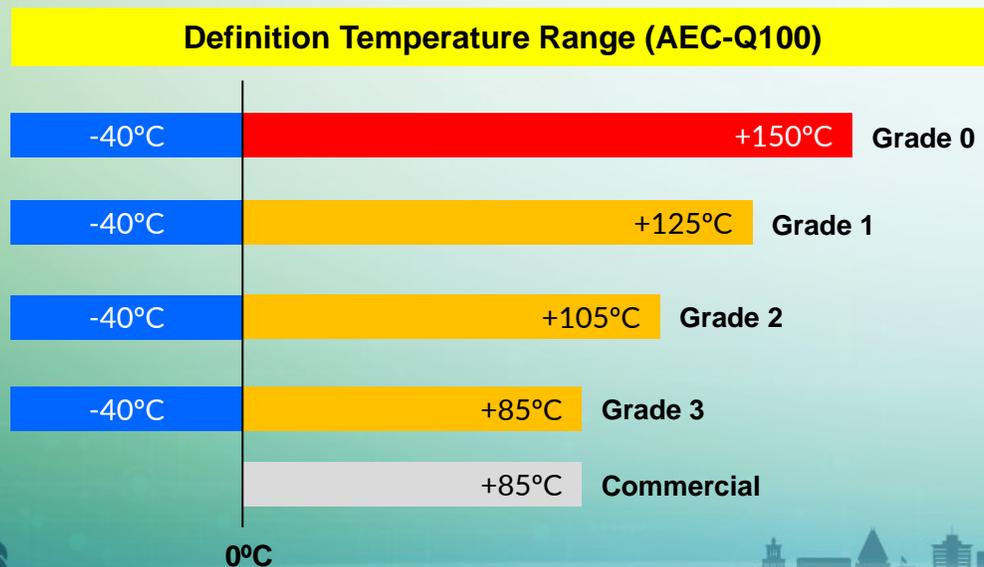


Alan Liao

2nd Annual SWTest Asia | Taiwan, October 17

Automotive grades and lifecycles

- **Automotive Temperature Grades**
 - 4 grades by temperature range. - 40°C to +85°C, +105°C, +125°C, +150°C
- **Additional process requirement**
 - Additional process steps to ensure the Quality and Reliability.
- **Special BOM consideration**
 - Special BOM to ensure the Performance and Lifecycles



Reliability Test at Wafer Level

- **Package Sort Test Item is moving to Wafer level Test**
 - WLBI (wafer level burn-in) at Sort Step, Test Items are enforced, Package yield is improved
- **Package Reliability Test Item is moving to Wafer level Reliability Test**
 - Improves memory device quality faster than package reliability step.
- **Reliability Items (Temperature related)**

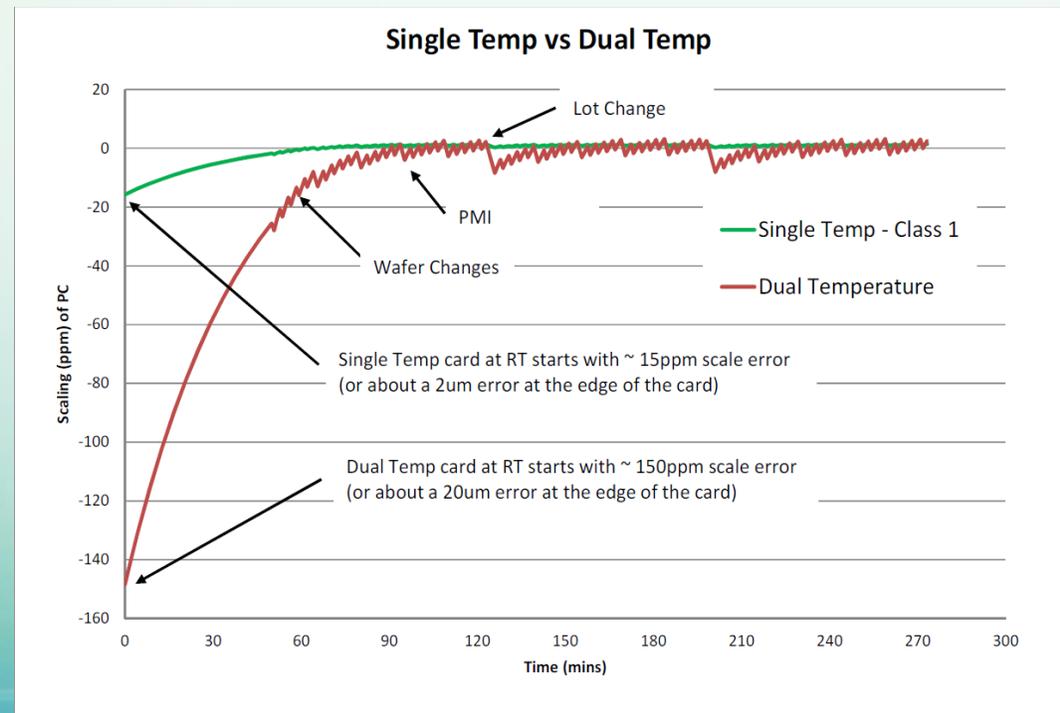
Stress	ABV	Test Method	Additional Requirement
Temperature Cycling	TC	JEDEC JESD22-A104 and Appendix 3	Grade 0: -55°C to +150°C for 2000 cycles or equivalent. Grade 1: -55°C to +150°C for 1000 cycles or equivalent. Grade 2: -55°C to +125°C for 1000 cycles or equivalent. Grade 3: -55°C to +125°C for 500 cycles or equivalent
Power Temperature Cycling	PTC	JEDEC JESD22-A105	Grade 0: Ta of -40°C to +150°C for 1000 cycles. Grade 1: Ta of -40°C to +125°C for 1000 cycles. Grades 2 and 3: Ta -40°C to +105°C for 1000 cycles.
High Temperature Operating Life	HTOL	JEDEC JESD22-A108	Grade 0: +150°C Ta for 1000 hours. Grade 1: +125°C Ta for 1000 hours. Grade 2: +105°C Ta for 1000 hours. Grade 3: +85°C Ta for 1000 hours.

Key Considerations for high temperature probe card design and manufacturing

- **Spring thermal stability**
 - Higher temperature capable spring material vs. current spring material
 - Spring repair process development
- **Interposer thermal stability**
 - IP temperatures from 125°C to 155°C depending on spring count
- **PCBA thermal stability and functionality**
 - PCBA temperatures from 110°C to 150°C depending on probe count
 - Material stability - Higher Tg material needed
 - Component operating temperatures – Capacitor, ADG, EEPROM, FPGA, Relay
- **DUTlet component**
 - DUTlet temperatures from 130°C to 160°C depending on probe count
 - Caps on DUTlets rated to 105°C/125°C typically

FormFactor High Temperature Solution

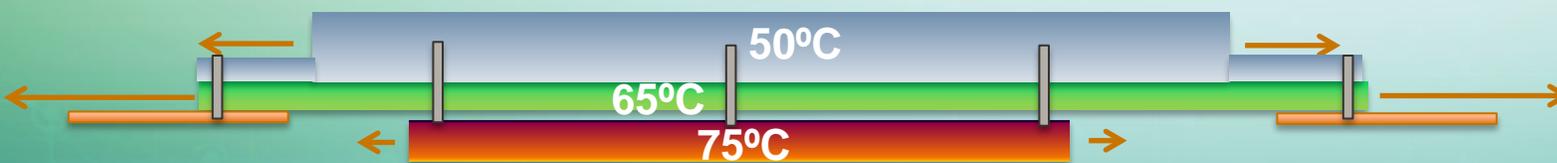
- Formfactor provides Dual Temp & Single Temp Probecards for high temperature demand
- Two types Spring – T11.2P for up to 130°C, T11.4P for >130°C
- Sophisticated Component selection considering high temperature on PCB



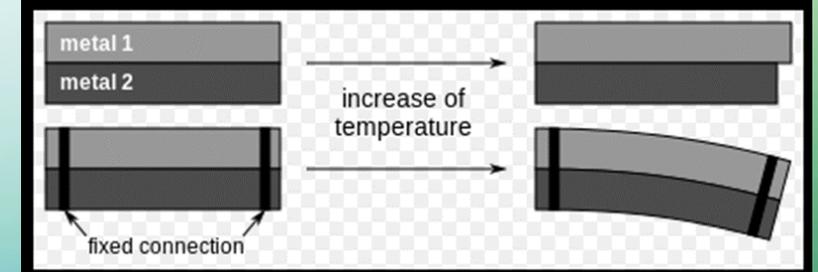
Wide Temp / Ultra High Temp Challenges

- **Thermal Z Behavior – to avoid thermal deflections**
 - Probe card Z movement is a function of many factors
 - Materials, Probe count, Cardholder material, Tester head interface, etc.
 - **Different CTE values** – TSS_(tester side stiffener), PCBA, WSS_(wafer side stiffener).
 - **Temperature difference by the location**
 - **WSS CTE** is selected to match the wafer expansion (dual temp), or to minimize expansion (single temp)
 - **TSS CTE** required to minimize Z movement at Hot/Cold.
 - The FormFactor Matrix card architecture has been extensively characterized and refined over hundreds of designs for many tester/prober combinations and has been optimized to provide industry leading thermal stability.

Example of Different Temperature, Different Expansion



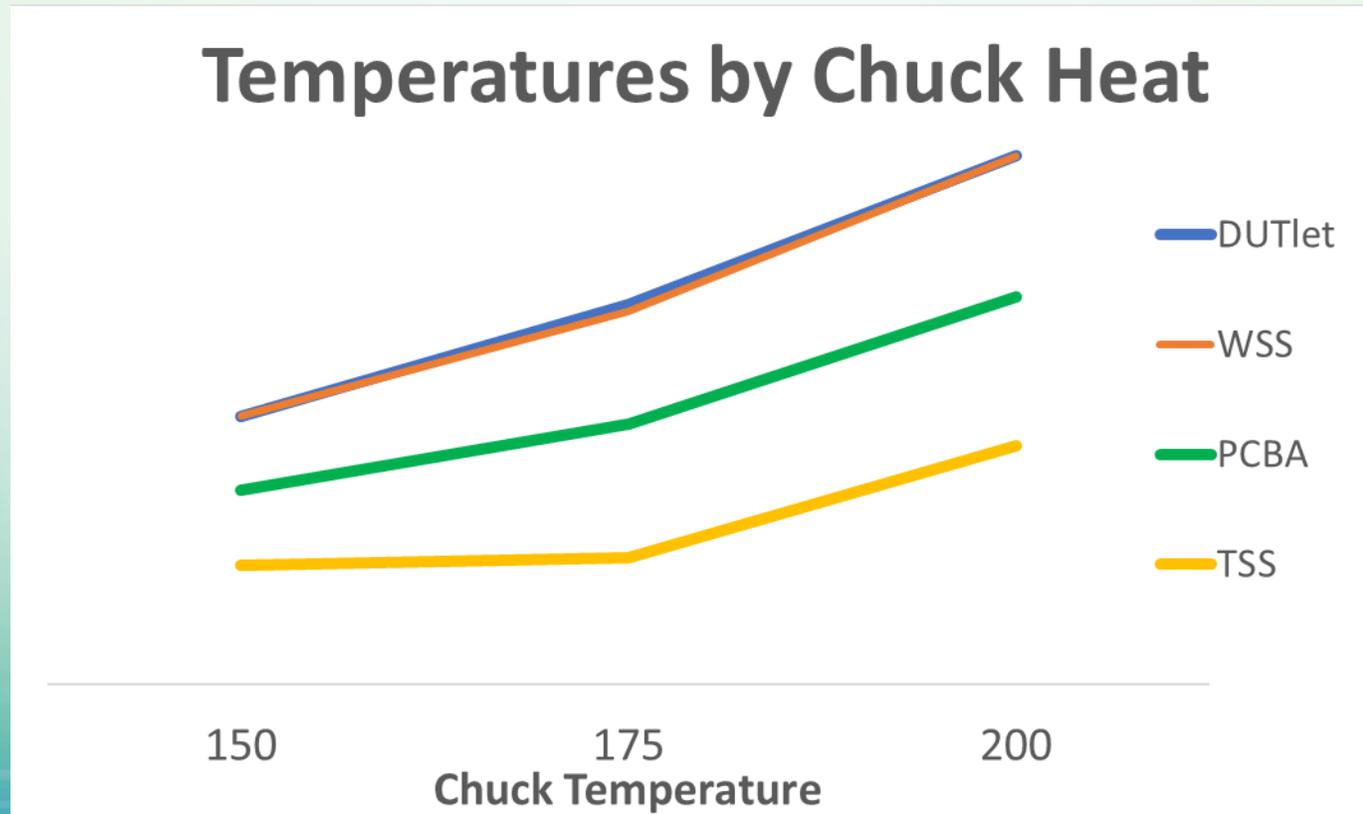
Thermal Deflection – vertically



Bimetallic strips curls when heated – different expansion ratio

Ultra High Temperature

- Thermal Characterization at 150/175/200°C
- Instrumented measurements of card temperatures at different chuck temperatures (15K spring Matrix probe card)



Grade-0 high parallel probecard development

- Objective

- To verify automotive **grade-0** (-40°C~+150°C) probecard **in main memory** device
- To verify the probecard running **at Reliability test condition** (>3 days wafer chip test condition)

- Card Test condition and check points

- To verify **stable contact mark** at +150°C wafer test condition
- To check **thermal movement for 72-hour** (3-day) contact test condition

Grade-0 high parallel probecard development

5 key considerations for 150°C memory wafer level test

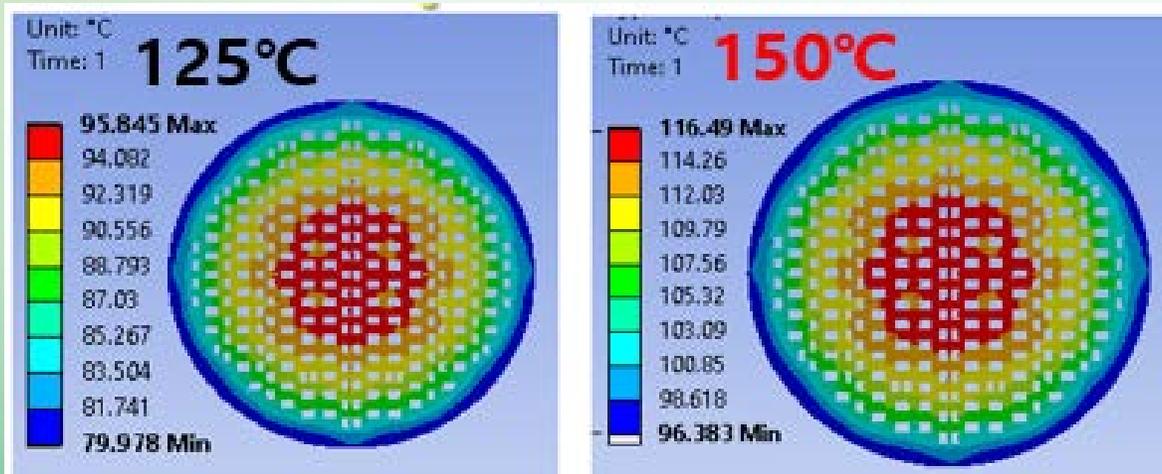
1. To decide **probing condition (soaking condition)** with different thermal uptake between probecard extraction and memory wafer at 150°C
2. Data error possibility at high voltage, high current test condition – probecard **component** burn-out or **degradation** check
3. Probe **contact stability at long test time (>72hours)** contact- Stable contact with >30% Pad edge margin (X, Y) and Z-direction stabilization within 1-hour.
4. To verify any system error or probecard damage possibility in **thermal cycling** (-40°C to 150°C or 150°C to 40°C)
5. To verify **probe life cycle at high stress** condition (high voltage/current) in long contact time condition for stable reliability data and probecard quality.

Memory Wafer Level Test Measurement -1

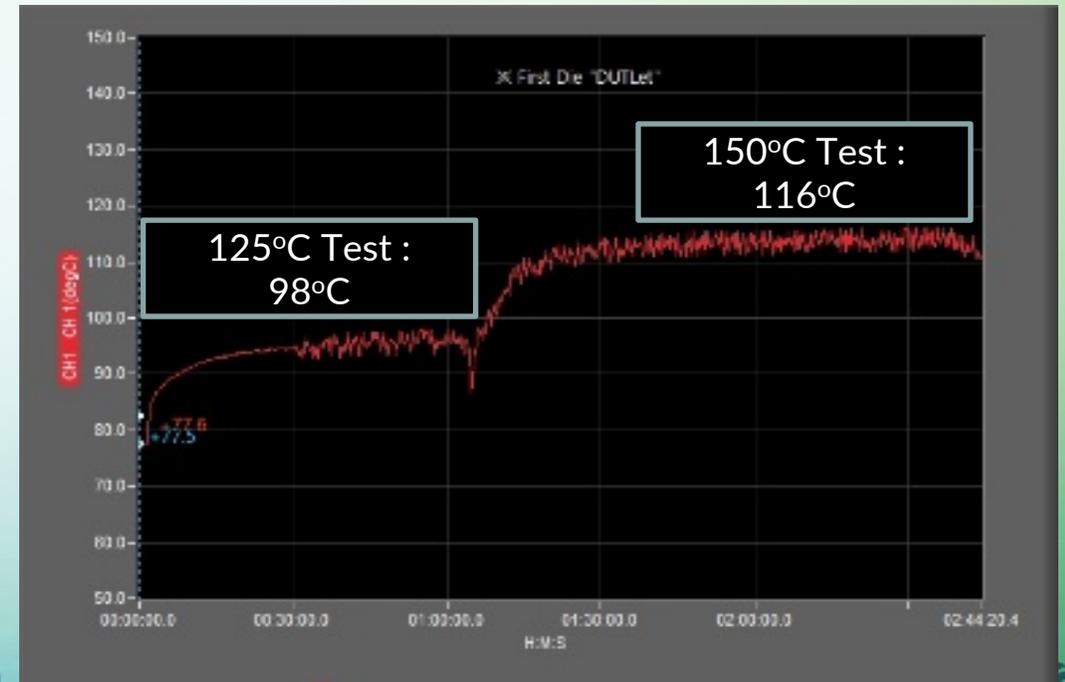
- Temperatures with non-operating condition

- Outlet (Contactor) temperatures at Chuck temperature 125°C and 150°C
- FFI simulation is matched with Samsung measurement

- Simulation at 125°C and 150°C



- Measurements at 125°C and 150°C



Memory Wafer Level Test Measurement -2

- Temperature measurement at memory device operating condition – with normal temp probecard
 - Considering over-heat, component should be placed outside chuck area
 - Heating components such as FPGA/Regulator/DC Relays are located outside chuck center – stable operation when wafer chip level test

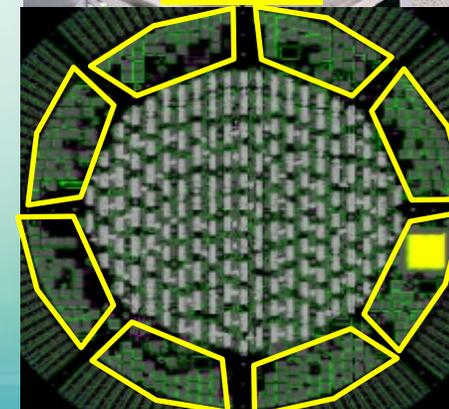
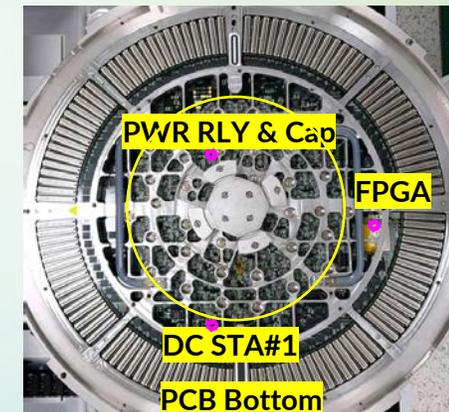
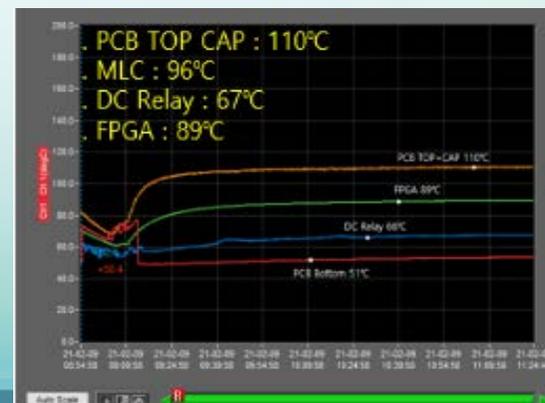
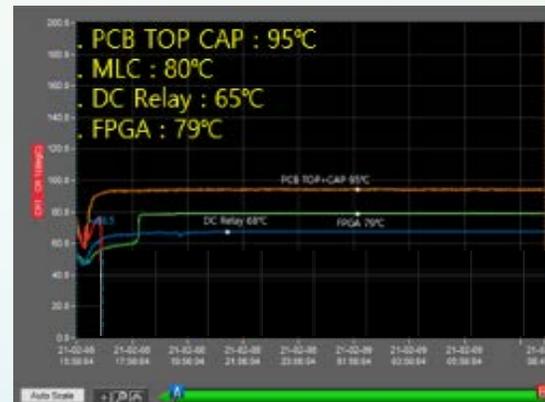
Standard Probecard



125°C Test

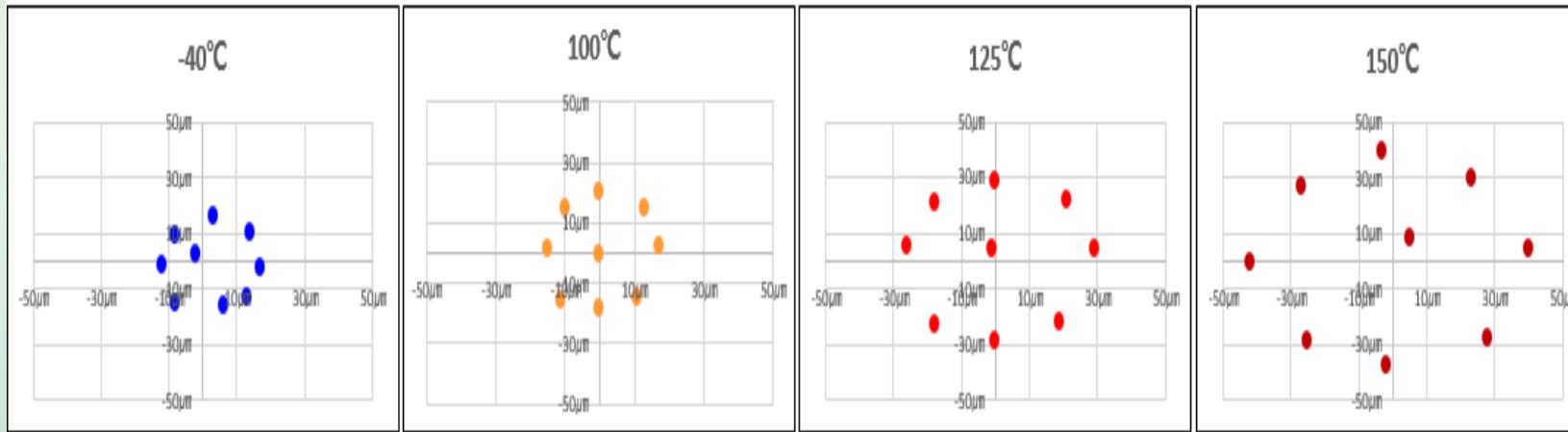
150°C Test

Grade-0 Probecard



Memory Wafer Level Test Measurement -3

- Contact Mark thermal movement

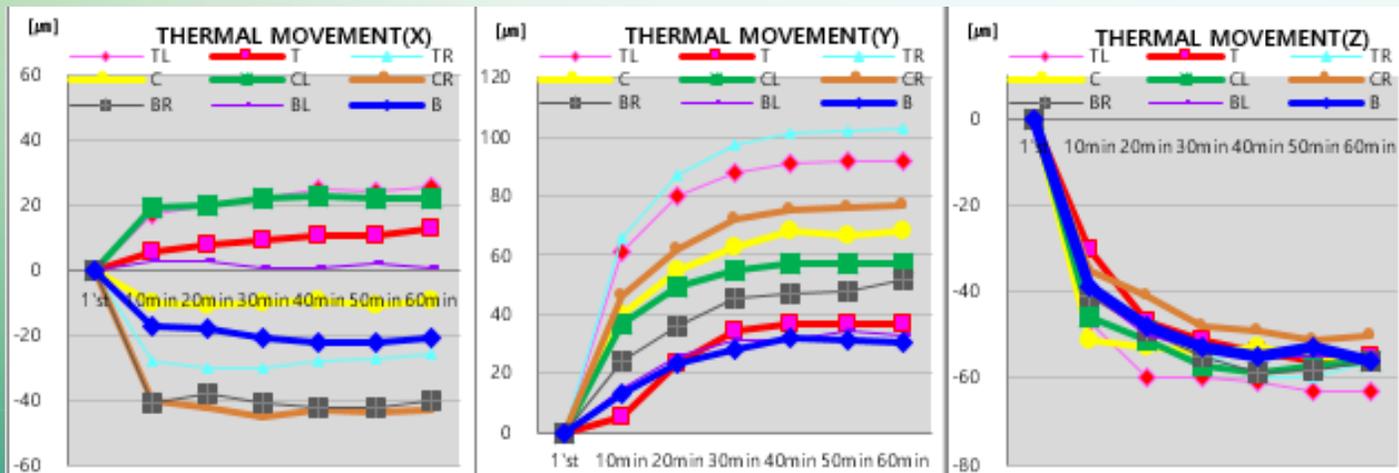


- Wafer PAD contact mark $\pm 14\mu\text{m}$ shrunken at -40°C and $\pm 40\mu\text{m}$ extracted at $+150^\circ\text{C}$
- These contact marks track the Silicon Wafer movement through this temperature range
- Proper probe offset and prober each cold and hot temp soak time. To make stable contact mark in PAD.

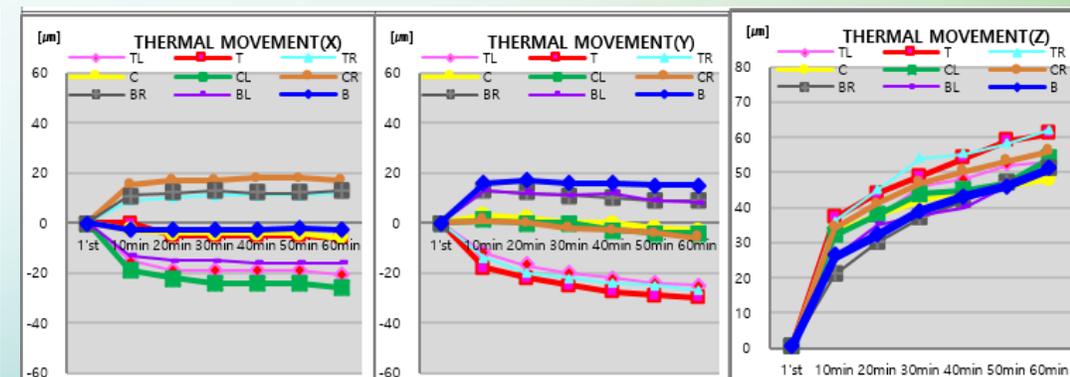
Memory Wafer Level Test Measurement -4

- XYZ thermal movements at Cold and Hot Test
 - Achieved stabilized contacts within an hour
- Result after 150°C 72 hours contact
 - Contacts are in 58% of PAD size, Achieved Pad edge margin >40%

HOT (150°C) THERMAL MOVEMENT (OD:180 μm)



COLD (-25°C) THERMAL MOVEMENT (OD:180 μm)



Achievement High Parallelism Memory Wafer Test Solution for High Temperature

	2015	2019	2021
FF Temperature	130°C	130°C	175°C
Samsung R&D	-25°C ~ 125°C	-25°C ~ 125°C	-25°C ~ 150°C
Probe card Parallel	HDT(X6TRE) 5TD @ 480mm	XDT(X16TRE) 2TD @ 520mm	HDT(X6TRE) 2TD @ 480mm
Probe Type	T11.2	T11.2	T11.4
Tip Force (gram force/mil)	0.8gf/mil	0.8gf/mil	0.8gf/mil
Probing Margin(%)	>±15%	>±15%	>±15%
Soak Time	60 min	20 min	20 min
Thermal offset	-2.4um / 0.3um	2.4um / 2.4um	-3um / 3um
Result of 1TD Probing	Qualified	Qualified	Qualified

Summary and Acknowledgements

- **Summary**

- Automotive Grade-0 Memory Wafer Level Test is feasible with High Parallel Probecard
- Memory Wafer Level Reliability Test (>72 hours contact test) at Grade-0 condition is feasible in PAD size with >40% PAD Edge margin.
- Maintain stable reliability data and probecard quality under probe lifecycle at high stress condition (high voltage/current) in long contact time condition.

- **Customer Acknowledgements**

- Jung Bae Ahn, Samsung Memory EDS Team

- **FormFactor Acknowledgements**

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Questions?

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THANK YOU

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