SWTEST
2021 CONFERENCE
PROBE TODAY,
FOR TOMORROW

30TH ANNIVERSARY

Next Generation KGD Memory Test Achieved Wafer Level Speed Beyond 3GHz/6Gbps

Byeongseon Ko
SK hynix, Engineering Director

Alan Liao (Speaker)
FormFactor, Director Probe BU Product Marketing

Aug. 30 – Sep. 1, 2021

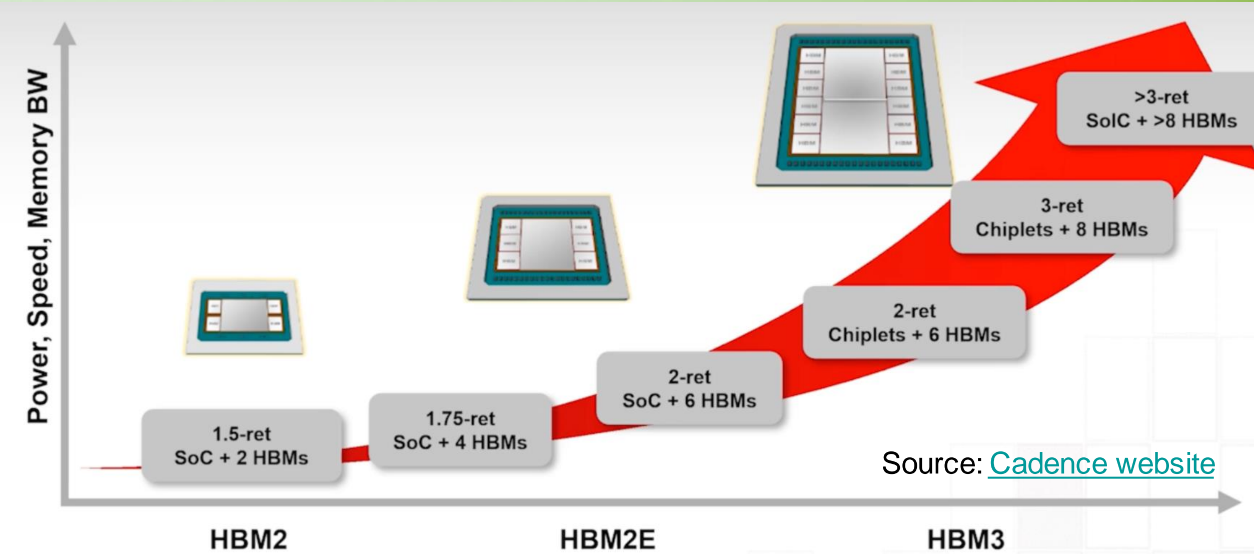
Agenda

- **Is Known Good Die/Stack Test Needed?**
  - Advanced packaging complexity trend
  - KGDS Tester Insertion in HBM manufacturing flow
- **KGDS test requirements challenge probe card design**
  - DRAM speed spec drives KGDS test speed requirement
- **Probe Card solution for KGD test**
  - Probe card solution case study: KGS HBM2 and KGD LPDDR4
- **Electrical Performance Validation**
  - Probe card design simulation & measurement vs. production test result
- **Feature Development Direction and Acknowledgement**
  - Conclusion, feature development and acknowledgement

Why DRAM KGDS Test Needed in Advanced Packaging?

- **Advanced Packaging Complexity Trend:**
  - From simple SoC + HBM to multiple SoC + multiple HBM
  - HBM DRAM stack increased
  - Package size growing
- **Advanced Packaging Revenue Growth in CAGR 6.6% (2014~2025)**
  - More chips in the package → high value $
  - Advanced Packaging offers more features and computing power than individual IC package result into market growth
- **DRAM KGDS Test Help Reduce Risk and Cost on Advanced Packaging/HBM**
  - Higher complexity → lower yield
  - Higher complexity → higher packaging cost
  - Earlier defect detection help save package cost

  https://www.swtest.org/swtw_library/2020proc/pdf/00pm_SWTest_Untethered_Keynote_Slessor_FormFactor.pdf



Wafer Test Coverage

Die Yield		Packaging Cost: Low	Packaging Cost: High
	High	Zero	Some
	Low	Some	Lots

Figure 2. Advanced Packaging market share evolution 2014-2025.

KGD Test: At Wafer Sort Test

DRAM Wafer

Wafer/TSV process

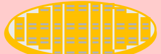
Flip

Thinning & Bump

dicing

wafer test

Logic



Wafer/TSV process

Flip

formation

stack & Mold

wafer test

ng

ebonding

KGS Test: Post-stack Wafer Test

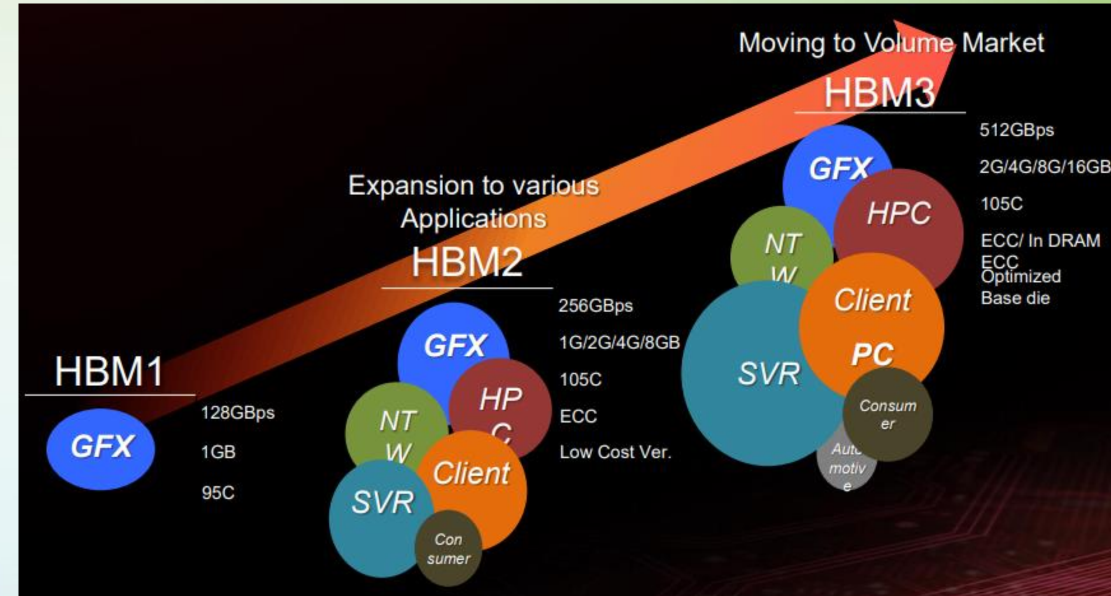
Shipment

KGS Test: Post-Stack Single Die Test

Where to Test in the	Test)	st)	Chioce 3 (Known Good Stack Single Die Test) DRAM Stack Die Post Dicing
	able to detect defects during wafer stack	ign to get Probing recipe optimization for wafer stack and material	HBM2 bump pitch and signal count challenge space transformer fan out (high cost) Probing recipe develop on single die stack handling

HBM and DRAM Data Rate Spec Drives KGD Test Requirement

- **HBM Application Expands to Broader Market**
  - From Graphic to Server, AI, Automotive, HPC
- **HBM to HBM3 Performance Enhancement**
  - Faster data rate speed
  - Higher memory bandwidth
  - Wider temperature range
- **KGD Test Requirements, PC Challenges**
  - Probe Card speed requirement from 1.6GHz to >3GHz
  - Temperature range from -40~125C to -40~150C
  - Test efficiency to meet high volume production

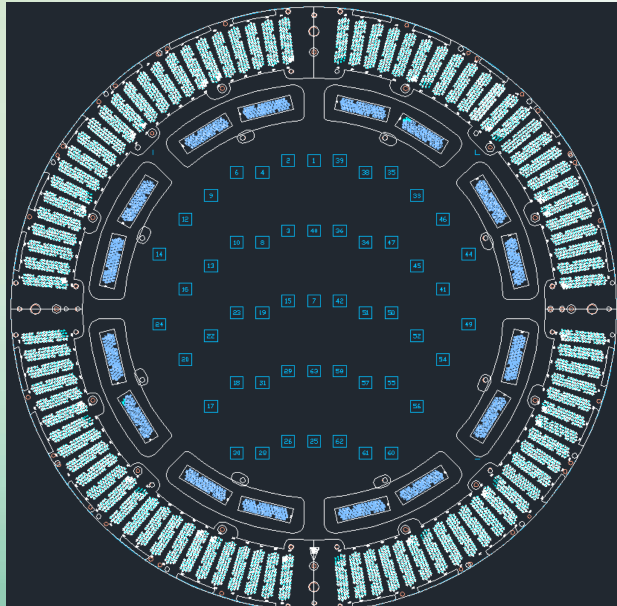


Source: SK Hynix Presentation "An In-depth Study of High Bandwidth Memory"

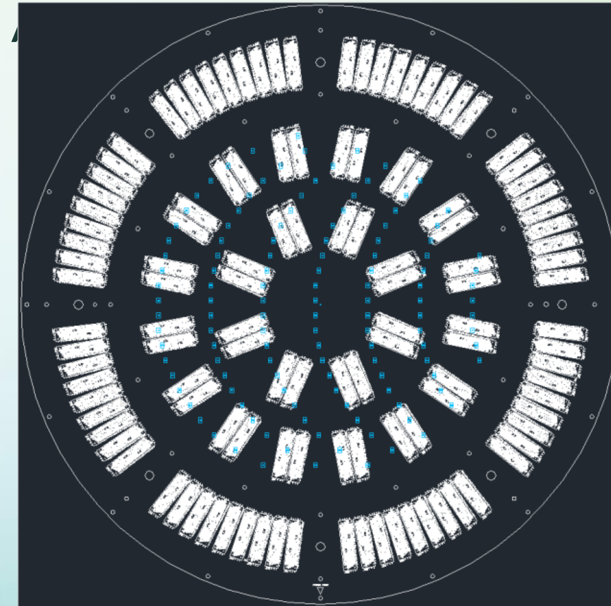
	DDR4	LPDDR4(X)	GDDR6	HBM2	HBM2E (JEDEC)	HBM3 (TBD)
Data rate	3200Mbps	3200Mbps (up to 4266 Mbps)	14Gbps (up to 16Gb ps)	2.4Gbps	2.8Gbps	>3.2Gbps (TBD)
Pin count	x4/x8/x16	x16/ch (2ch per die)	x16/x32	x1024	x1024	x1024
Bandwidth	5.4GB/s	12.8(17)GB/s	56GB/s	307GB/s	358GB/s	>500GB/s
Density (per package)	4Gb/8Gb	8Gb/16Gb/2 4Gb/32Gb	8Gb/16Gb	4GB/8GB	8GB/16GB	8GB/16GB/ 24GB (TBD)

Probe Card Solutions Case Study: KDS HBM2 and KGD LPDDR4

- **KGS HBM2 Probe Card**
  - Max 64DUTs, 18TD, T11.2P (-40~150°C)
  - Target Speed 3.2GHz
  - Advantest T5503 HS2 H7-010508



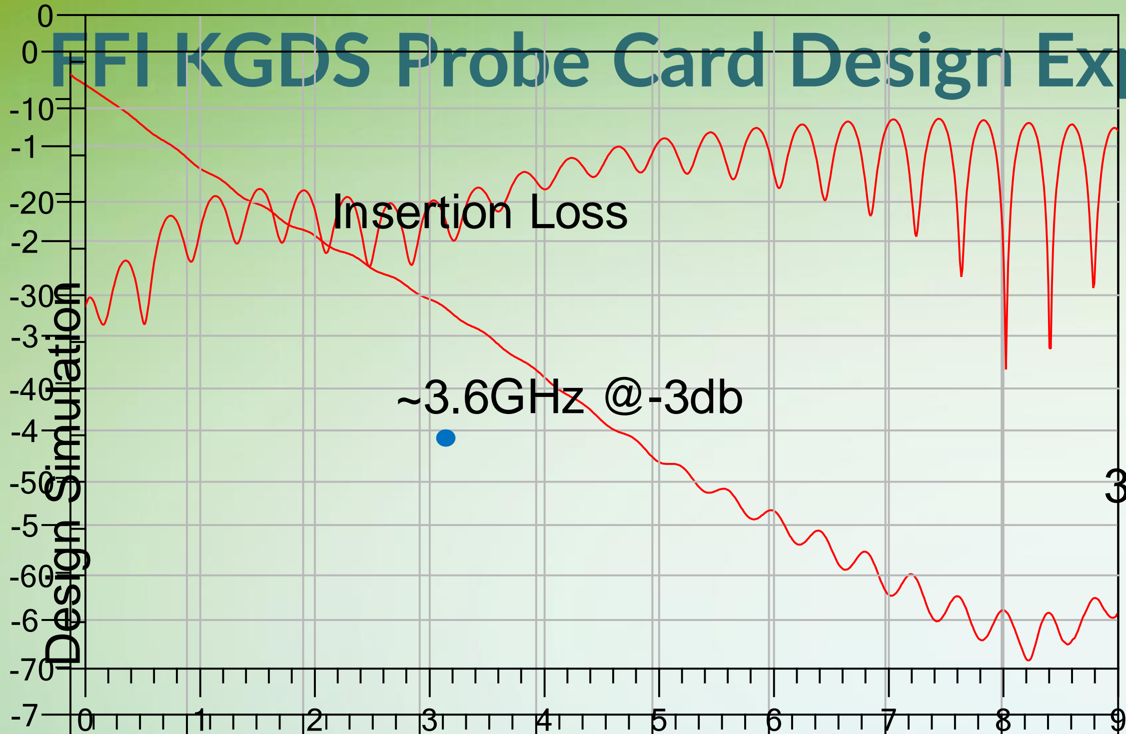
- **KGD LPDDR4 Probe Card**
  - Max 128DUTs, 45TD, T11.2P (-40~150°C)
  - Target Speed 3.2GHz
  - -010569

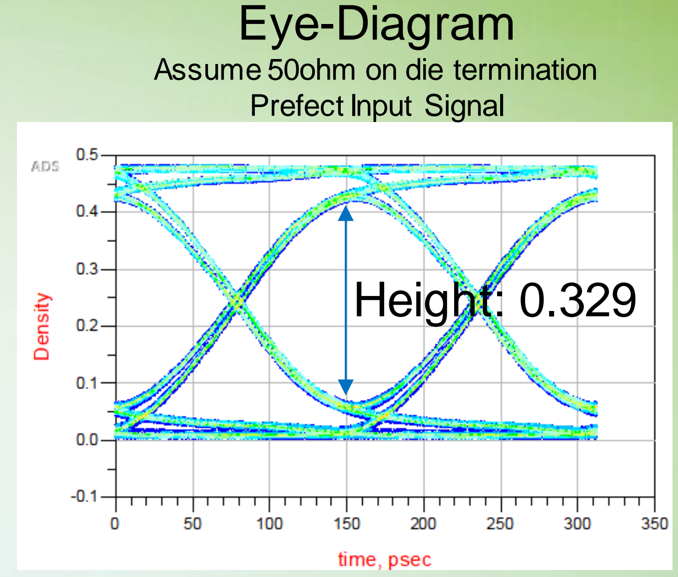


Both Probe Card Solution Achieve Highest DUT Parallelism and Speed Requirement (>3GHz), T11.2P Offers Wide Temperature Range

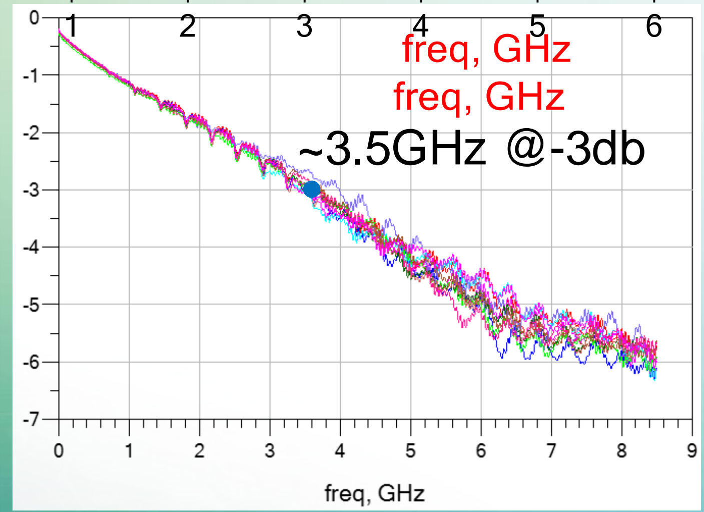
FFI KGDS Probe Card Design Experience: Design & Actual Correlated

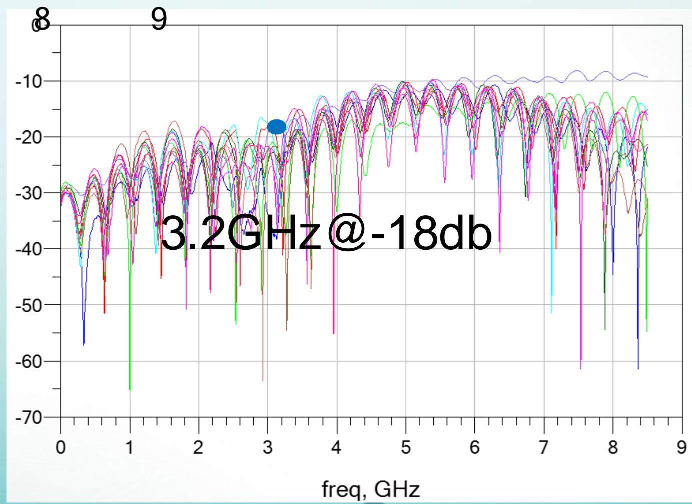
Design Simulation

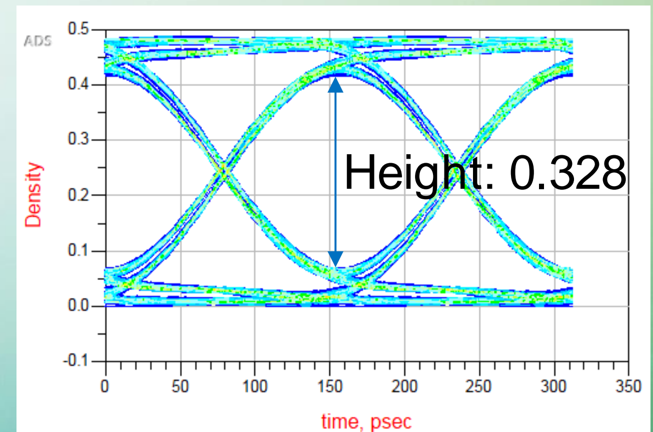




Outgoing Measurement







KGD LPDDR4 Probe Card SHMOO Result

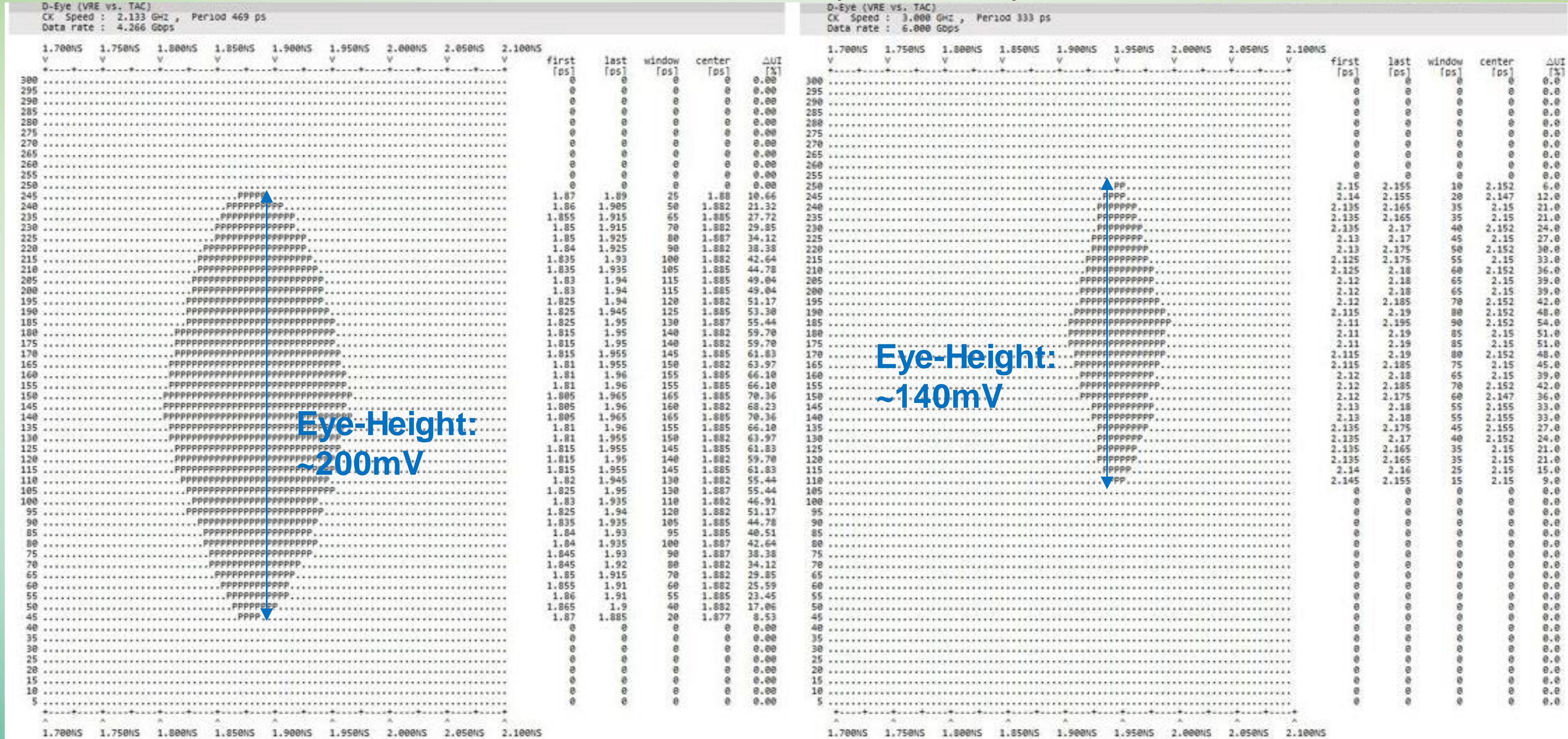
```
          SHMOO (TCK vs. TAC)
          PATTERN :  (B16+B16Inv)X3X8X2
          VDD     :  1.020V

             2.400NS   2.450NS   2.500NS   2.550NS   2.600NS   2.650NS   2.700NS   2.750NS   2.800NS
Speed        v         v         v         v         v         v         v         v         v  P-count  Ideal UI    UI    ΔUI
[Gbps]  [ps] +----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+   [ # ]      [ps]  [ps]    [%]
 4.000   500 .................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP............................      36     250.0   180   72.0
 4.040   495 .................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP..............................      34     247.5   170   68.7
 4.082   490 ...................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP............................      34     245.0   170   69.4
 4.124   485 ...................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP.............................      33     242.5   165   68.0
 4.167   480 .....................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP...........................      33     240.0   165   68.8
 4.211   475 ......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP............................      31     237.5   155   65.3
 4.255   470 .......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP...........................      31     235.0   155   66.0
 4.301   465 .......................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPPP...........................      31     232.5   155   66.7
 4.348   460 ........................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP............................      29     230.0   145   63.0
 4.396   455 .........................PPPPPPPPPPPPPPPPPPPPPPPPPPPPPP..........................      30     227.5   150   65.9
 4.444   450 ..........................PPPPPPPPPPPPPPPPPPPPPPPPPPPPP..........................      29     225.0   145   64.4
 4.494   445 ...........................PPPPPPPPPPPPPPPPPPPPPPPPPPPP..........................      28     222.5   140   62.9
 4.545   440 ............................PPPPPPPPPPPPPPPPPPPPPPPPPP.P.........................      27     220.0   135   61.4
 4.598   435 .............................PPPPPPPPPPPPPPPPPPPPPPPPPP..........................      26     217.5   130   59.8
 4.651   430 ..............................PPPPPPPPPPPPPPPPPPPPPPPPPP.........................      26     215.0   130   60.5
 4.706   425 ...............................PPPPPPPPPPPPPPPPPPPPPPPPPP........................      26     212.5   130   61.2
 4.762   420 ...............................PPPPPPPPPPPPPPPPPPPPPPPP..........................      24     210.0   120   57.1
 4.819   415 ................................PPPPPPPPPPPPPPPPPPPPPPPPP........................      25     207.5   125   60.2
 4.878   410 ..................................PPPPPPPPPPPPPPPPPPPPPPPP.......................      24     205.0   120   58.5
 4.938   405 .................................PPPPPPPPPPPPPPPPPPPPPPPP........................      24     202.5   120   59.3
 5.000   400 ...................................PPPPPPPPPPPPPPPPPPPPPP........................      22     200.0   110   55.0
 5.063   395 ...................................PPPPPPPPPPPPPPPPPPPPPPP.......................      23     197.5   115   58.2
 5.128   390 ...................................PPPPPPPPPPPPPPPPPPPPPP........................      22     195.0   110   56.4
 5.195   385 .....................................PPPPPPPPPPPPPPPPPPPPPP......................      22     192.5   110   57.1
 5.263   380 ......................................PPPPPPPPPPPPPPPPPPPP.......................      20     190.0   100   52.6
 5.333   375 ......................................PPPPPPPPPPPPPPPPPPPPPP.....................      22     187.5   110   58.7
 5.405   370 ........................................PPPPPPPPPPPPPPPPPPPP.....................      20     185.0   100   54.1
 5.479   365 .........................................PPPPPPPPPPPPPPPPPP......................      18     182.5    90   49.3
 5.556   360 ..........................................PPPPPPPPPPPPPPPPP......................      17     180.0    85   47.2
 5.634   355 ..........................................PPPPPPPPPPPPPPPPPP.....................      18     177.5    90   50.7
 5.714   350 ............................................PPPPPPPPPPPPPPPP.....................      16     175.0    80   45.7
 5.797   345 ...........................................PPPPPPPPPPPPPPPP......................      16     172.5    80   46.4
 5.882   340 ..............................................PPPPPPPPPPPPPP.....................      14     170.0    70   41.2
 5.970   335 ..............................................PPPPPPPPPPPPPP.....................      14     167.5    70   41.8
 6.061   330 ...............................................PPPPPPPPPPPPPP....................      14     165.0    70   42.4
 6.154   325 .................................................................................       0     162.5     0    0.0
 6.250   320 .................................................................................       0     160.0     0    0.0
 6.349   315 .................................................................................       0     157.5     0    0.0
 6.452   310 .................................................................................       0     155.0     0    0.0
 6.557   305 .................................................................................       0     152.5     0    0.0
 6.667   300 .................................................................................       0     150.0     0    0.0
             +----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+----+
             ^         ^         ^         ^         ^         ^         ^         ^         ^
             2.400NS   2.450NS   2.500NS   2.550NS   2.600NS   2.650NS   2.700NS   2.750NS   2.800NS
```

- **SHMOO Plot from Tester on TCK vs. TAC Pin at 105°C Test**
  - LPDDR4 KGD test target spec 4.266Gbps (~2.2GHz)
  - Maximum test speed run up to 6.061Gbps (~3.0GHz)
  - Test pattern total # of transition >1632 times
  - Test pattern considered ISI (inter symbol interference)
- **Conclusion:**
  - From 2GHz speed to 3 GHz speed test all patterns passed enough timing margin
  - From 2GHz to 3 GHz, probe card degradation within 25ps only. Exceeds expectation.
  - FFI K32 probe card proven works beyond 3GHz speed test

KGD LPDDR4 Probe Card D-Eye SHMOO Result

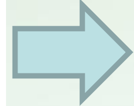
D-Eye (VRE_OUT vs. TAC) SHMOO
Data Rate 4.266Gbps and 6Gbps

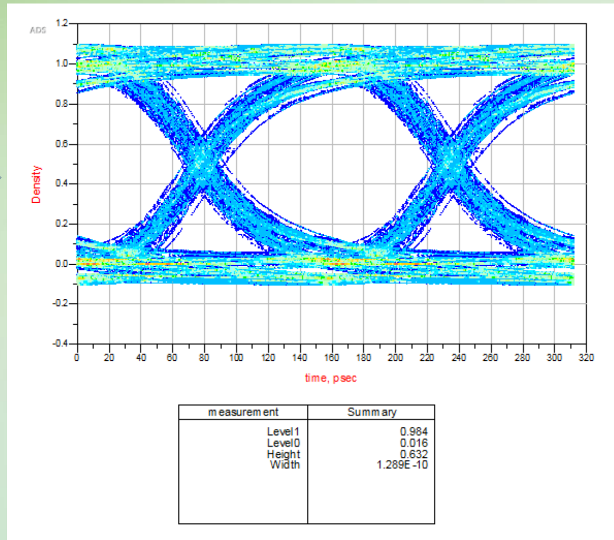


- At 3GHz data rate, eye-height achieve ~40% good margin for KGD test

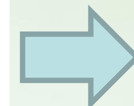
LPDDR4 Probe Card D-Eye SHMOO Conclusion

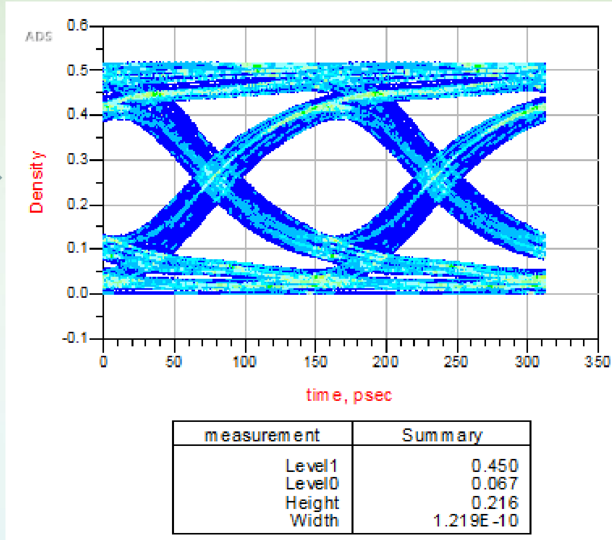
Perfect Input Signal



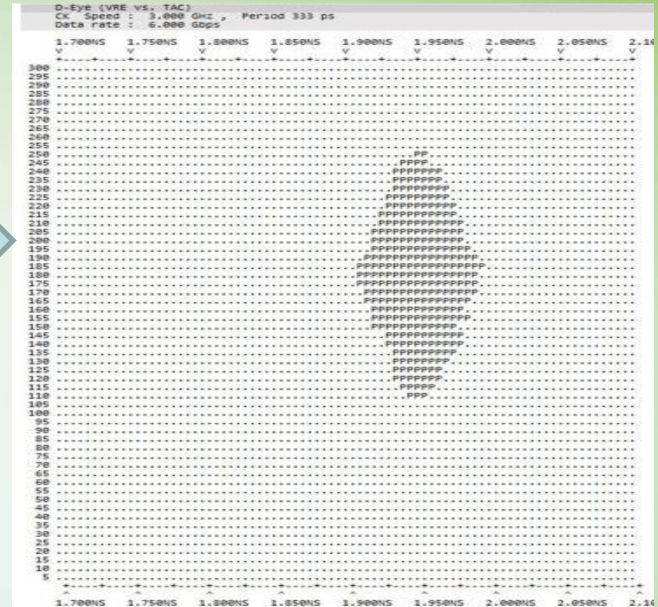


Tester Input Signal Simulation 3.2GHz





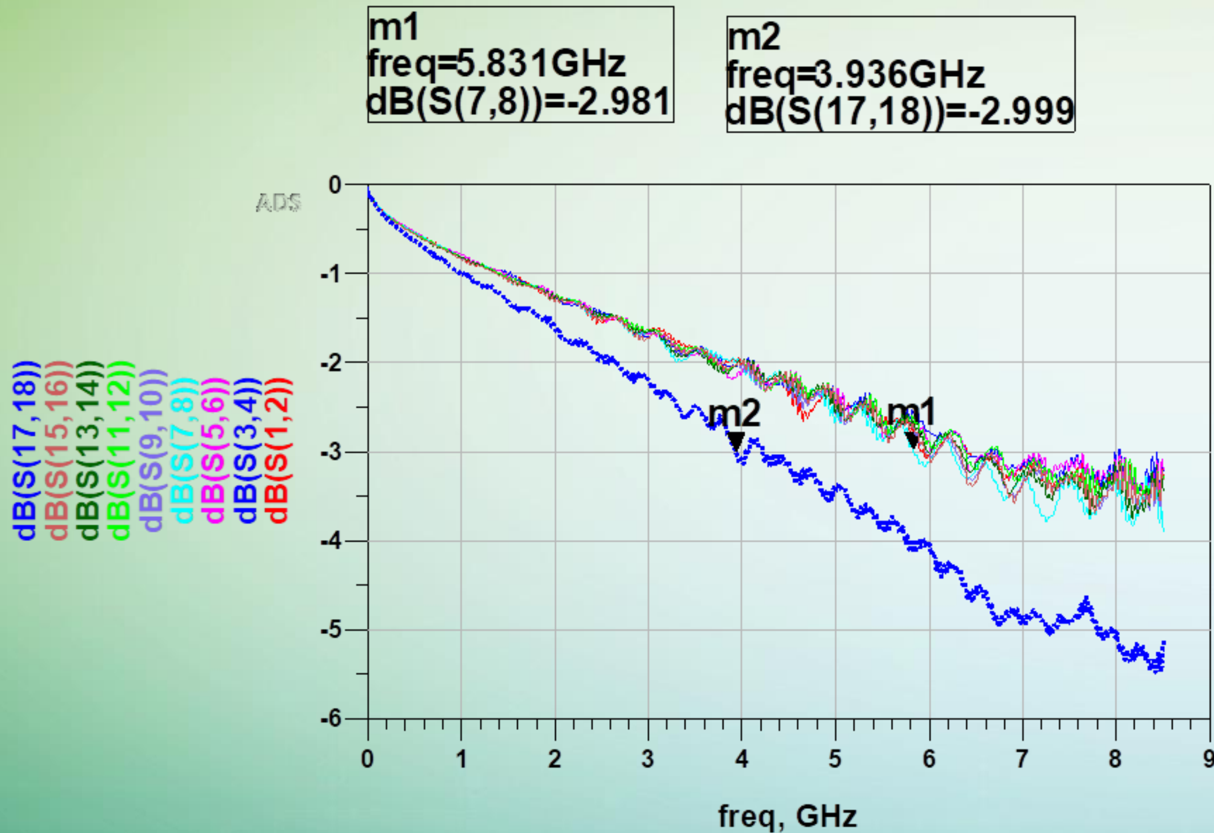
Probe Card Output Simulation 3.2GHz



D-Eye SHMOO from Test Floor 3.0GHz Data Rate Test Pattern

- FFI simulation considered tester and probe card signal degradation
- Simulation considers ideal case (no crosstalk noise and power/GND noise)
- Simulation shows 43% eye height, confirmed by SHMOO plot and test floor data, performance reach 90~95% to the simulation result.
- Both simulation and actual test result show FFI K32 probe card capable for >3GHz test speed, correlate between design simulation and test result

Further Improve Probe Card Speed Performance Beyond 4GHz Specification



M1: PCB design with Advanced Design Rule
M2: PCB design with HFTAP K32 Design Rule

- **FFI PCB Design Measurement Result Show There is Path for Probe Card Support >5GHz KGDS Test Requirement**
  - Multiple signal channel PCB only simulation
  - With advanced design rule (for HFTAP K40 and K50 product)
  - Existing tester configuration
  - With PCB high speed material and manufacturing rule
  - -3dB bandwidth improve by 1.9GHz

Future KGDS Probe Card Development Direction

- **Satisfy for Higher Speed Test Requirements**
  - K32 (3.2GHz) has released to HVM
  - K40 (4.0GHz) in customer evaluation
  - Probe Card architecture proven for >5.0GHz speed
  - >4.0GHz development pending ATE roadmap
- **Increase Test Efficiency by Raising Maximum # of DUT on Probe Card**
  - K16 (1.6GHz) has a solution for x2 signal sharing by x2 TTRE technology t double the parallelism
  - Co-working with tester companies for higher density channels for x256 DUT at 3.2GHz ~ 4.0GHz solutions

Memory KGDS Speed Test Requirement vs. FFI Product Line

FFI Product Platform	FFI HFTAP Product Class	Clock (MHz)	Data Rate (Mbps)
		8000	16000
		7000	14000
		6400	12800
		5600	11200
Matrix	K40	4267	8533
		3733	7466
Matrix	K32	3200	6400
		2800	5600
Matrix	K22	2134	4267
		1867	3733
Matrix	K16	1600	3200
Matrix	K12	1339	2677
Matrix	K10	1067	2133
		933	1866
Matrix, PH	K8	800	1600
		667	1333
Matrix, PH	K5	534	1067
HVM	Customer Eval	R&D: Pending ATE	

Key Take Aways and Acknowledgments

- **KGDS Test Demand Increase as Advanced Packaging (HBM) Chip demand Increases Dramatically**
  - AP IC revenue continues growing since 2014 forecast at 6.6% CAGR
  - As more IC integrate to AP and size & signal channel scale, AP become more complex which leads to a low yield and high-cost combination.
  - KGDS test is one way to improve final yield and reduce packaging cost by eliminating bad components at early packaging stages
- **KGDS Test Requirements Continue to Challenge Probe Card Technology**
  - KGDS test speed requirement continues to increase (from 800MHz to 3.2GHz)
  - As AP IC demand increases, KGDS test solution requires better test efficiency to reduce cost and support higher volume
  - FFI HFTAP probe card technology has validated on production test passed 3.0GHz speed and achieved max 128 DUT. Performance and measurement data show promising result on Probe Card support higher speed and parallelism

- **Acknowledgment**
  - Mr. Byeongseon Ko (SK hynix): worked with FFI provided production test data
  - Mr. MJ Lee (FFI): provided materials for this presentation
  - Mr. Jim Tseng (FFI): provided simulation & measurement data for this presentation