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30TH ANNIVERSARY

Next Generation SmartMatrix Probe Card Technology Enables 3000-Parallelism 1TD Test for D1z/D1a DRAM Process Node

FormFactor™

SAMSUNG

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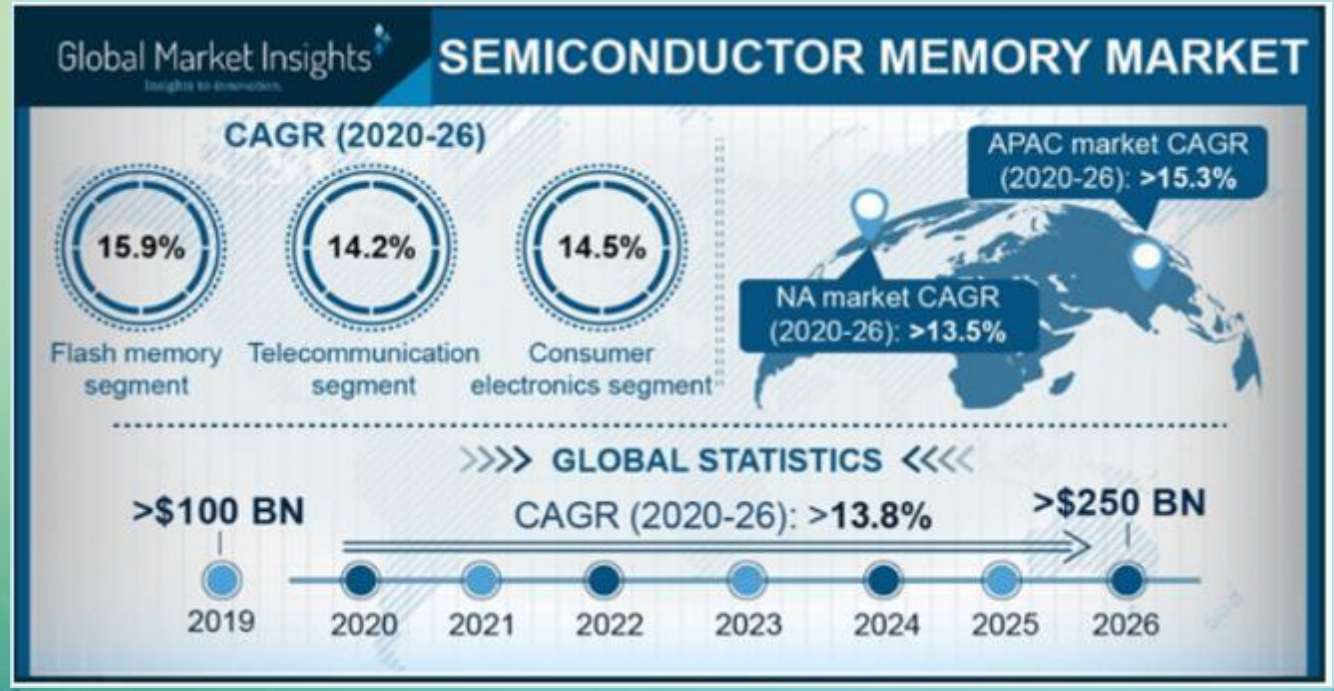
SmartMatrix 3000XP: Agenda

- Semiconductor memory market demand
- 1-Touchdown wafer test efficiencies
- SmartMatrix 3000XP features and benefits
- Technical challenges solved and performance feedback
- Summary and Acknowledgements

Strong Memory Market: Continued Growth

- **DRAM demand has been strong through 2020-2021, expect to continue with applications growth**



Leading IC Product Segments in 2020
Sales and Revenue Growth

Rank	Sales	$M	Revenue Growth	20/19 % Chg
1	DRAM	$65,215	NAND Flash	25%
2	NAND Flash	$55,154	Cellphone Application MPUs	24%
3	Computer CPU	$43,848	Wired Comm—Spcl Purp Analog	20%
4	Computer and Periph—Spcl Purp Logic	$31,340	Computer and Periph—Spcl Purp Logic	15%
5	Cellphone Application MPUs	$26,615	Wireless Comm—Spcl Purp Logic	12%

Source: IC Insights — Rankings apply to IC product categories with more than $100M in annual sales.

DRAM Industry Growth Prospect

- 2021-2026 9.7% CAGR
- ~$65BN → ~$110BN

Source: MarketWatch Aug '21

DRAM Key Applications

- Server/big data
- Mobile devices
- PC

Advancement of Die Per Wafer (DPW)

- Latest process nodes support die shrink, leading to more die per wafer
- As density grows, die may become larger, but continued nodes drive increase in DPW.

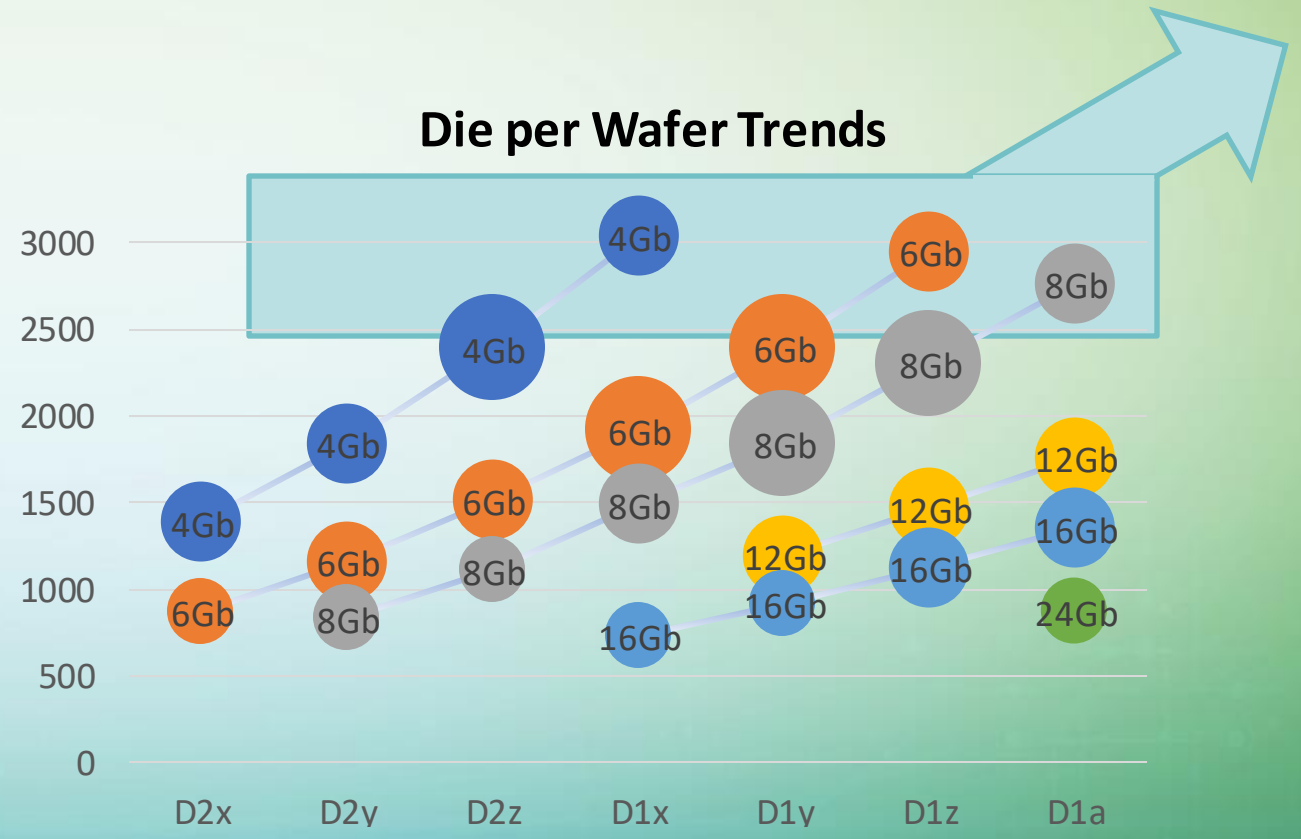
DRAM Process Roadmaps (for Volume Production)

	2015	2016	2017	2018	2019	2020	2021
Samsung		1xnm		1ynm		1znm	1αnm	1β
SK Hynix		21nm		1xnm	1ynm	1znm	1αnm	
Micron		20nm	1xnm		1ynm	1znm	1αnm	1β
CXMT						1xnm		1ynm

Source: IC Insights

	YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
DRAM	*Calculated from above*						
4G	Chip size (mm)	2.7					
	DPW (cell size*Bit/chip on 300mm)	2908	-	-			
8G	Chip size (mm)	3.8	3.3	2.7			
	DPW (cell size*Bit/chip on 300mm)	1,777	1,952	2,969			
12G	Chip size (mm)	4.7	4.1	3.3	2.6		
	DPW	969	1,301	1,979	3,092		
16G	Chip size (mm)	5.4	4.7	3.8	3.0		
	DPW	727	976	1,484	2,319		

Source: The IRDS 2020



1TD Wafer Test for Highest Efficiency

- **A 1TD Probecard tests all devices on wafer with a single touchdown**
- **Why is 1TD Wafer Test desirable?**
  - Highest wafer throughput, maximize test cell capacity
  - Do more with less capital equipment (smaller factory / footprint needed!)
  - Well-supported with recent demand.

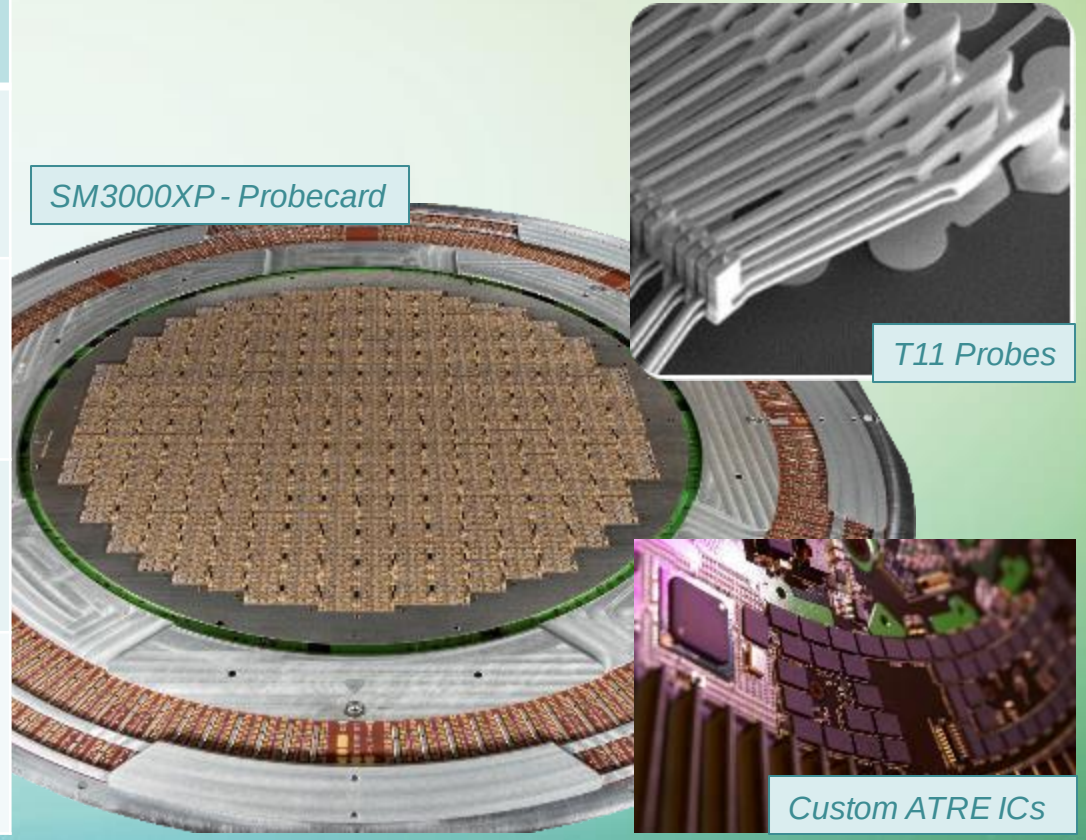
- **Time benefit (1TD vs 2TD example)**
  - Overall Wafer Test Time reduced by 33%. This is a 50% test cell throughput increase

- **Challenge: Maintain 1TD probe card capability as DPW continues to increase**

SmartMatrix 3000XP: 1TD 3000DPW Probe Card

- **SM3000XP is an extension of the proven SmartMatrix probe card developed for high probe count, high parallelism, high density designs**

SM3000XP Key Features	SM3000XP Benefits
FFI High Density ICs ATRE ASICs, FET modules	**Resolves part placement constraint** Enable physical placement of the required components to address the >3000 parallelism requirement
FFI TTRE Terminated TRE module and test solution	**Lower cost of test** FFI proprietary termination solution enables tester resource sharing of up to 32 times while maintains signal performance on existing testers
High-probe count and Density 3D-MEMS springs on DUTLet	**Shorter lead time** Lithographically mount hundreds and thousand of probes on die as opposed to single probe bonding to substrate
Thermo-mechanical stability High-range dual temp use	**Stability across temperature range** T11 MEMS spring with stable coplanarity across up to 170C temperature range (-45C to 125C, typical. 150C max)



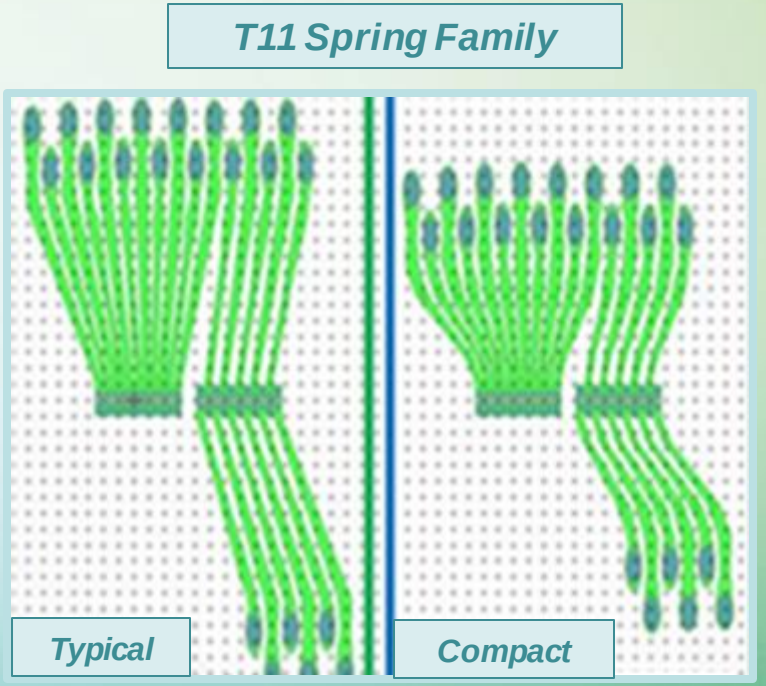
Key Challenges Solved for SM3000XP

1. **Probe density:** >160,000 total probes on small device
2. **PCB routing/component density:** support for >40,000 nets and components
3. **Signal integrity and PDN:** maintain speed and amplitude with sharing
4. **Mechanical Optimization:** must support existing probe card test cell
5. **Probe mark Pad Size Capability:** achieve scrub marks within keepout across dual temperature test range

Probe density: >160,000 total probes on small device

- **Developed a "compact version" of the T11 field proven probe**
  - Less than 1.5mm length probe supporting 4mm die sizes or smaller

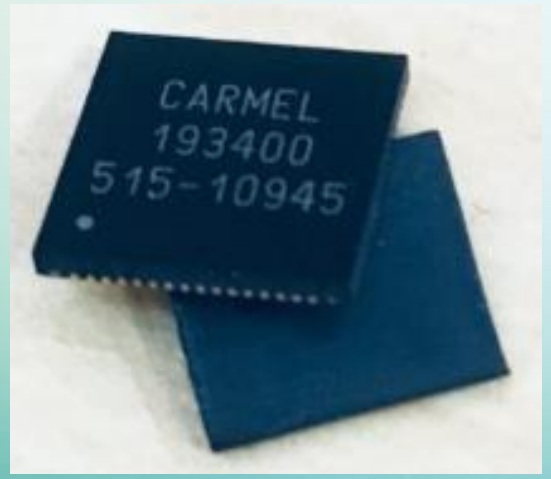
Compact T11 Spring Technology
T11 compact probe developed in order to physically fit all ~160,000 probes into the 300mm active area of small devices
Probe force reduced by ~10% for 450kg chuck force of existing high probe count test cells.
Same T11 max overtravel (125um AOT) for a wide overdrive operating window for stable production



PCB Routing / Component Density

- **Need to fit more technology in same probecard space**
- **Developed more compact and higher density switches and FETs**
- **ATRE share increased from x16 and x32 enables throughput increase**
  - 96 site ATE tester can achieve up to 3072// with x32 share
- **Improved component placement precision on FFI processes**

FFI Carmel 2XDC Boost
Double-density 128-Switch per Package

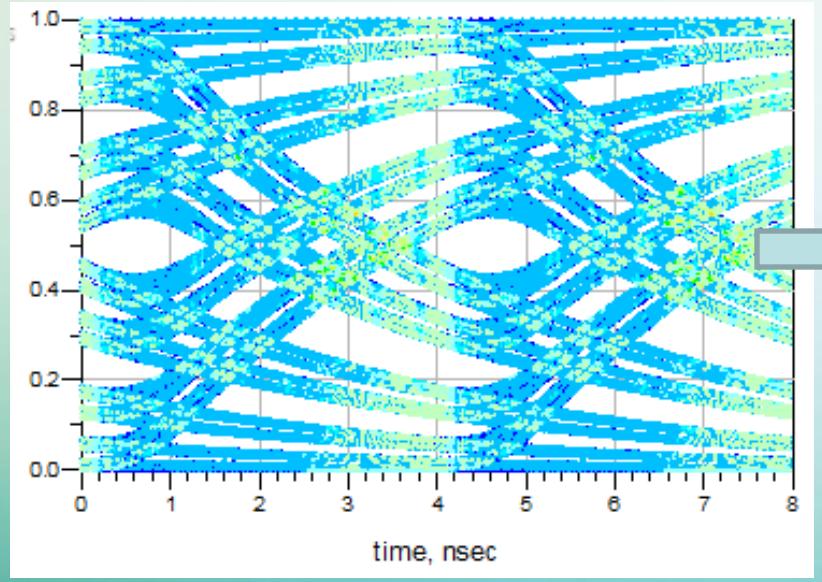


FFI PPS TRE x8 FET
50% Area Reduction

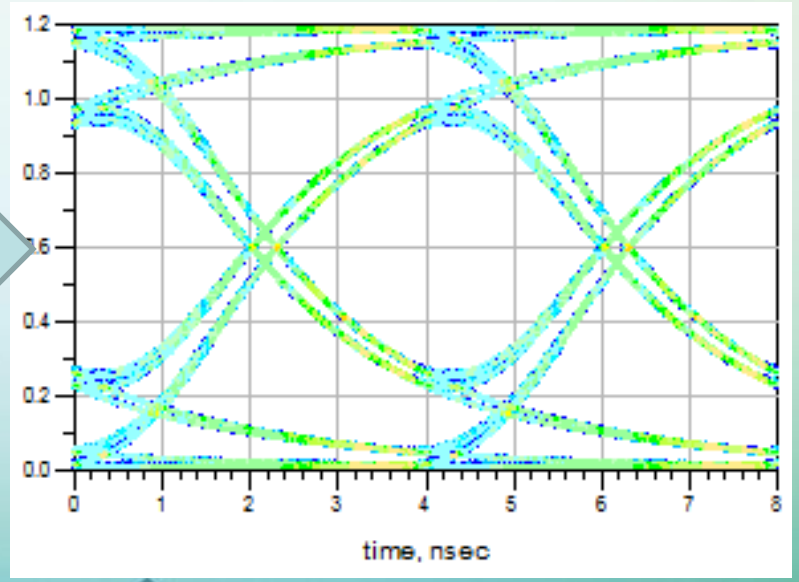
SM3000XP x32 TTRE Simulation

- **SI must be capable despite extended resource sharing**
- **TTRE (terminated TRE) - termination improves signal reflection noise at the share point, increases signal amplitude, test speed is not compromised**
  - X32 probe card SI simulated performance with and without
  - Without TTRE, the transient amplitude for x32-TRE share is not sufficient

Without TTRE



With TTRE

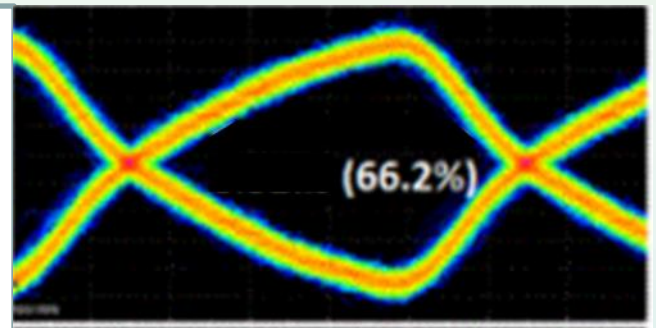


Signal Performance result – Samsung

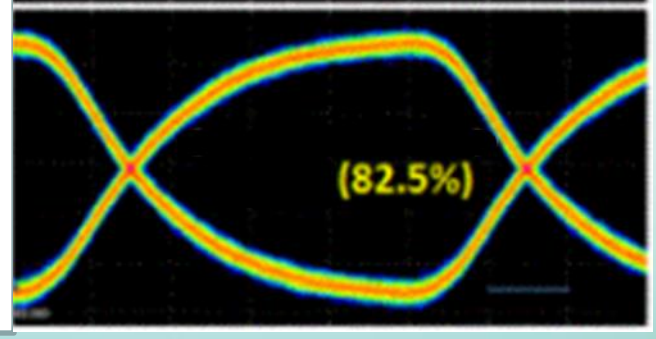
- **Extending Fan-Out / Sharing to X32:** Signal transmission loss is compensated with FormFactor's ASIC.

SI Performance Measurement Result

X32 Margin = 66.2%
TTRE OFF



X32 Margin = 82.5%
TTRE ON

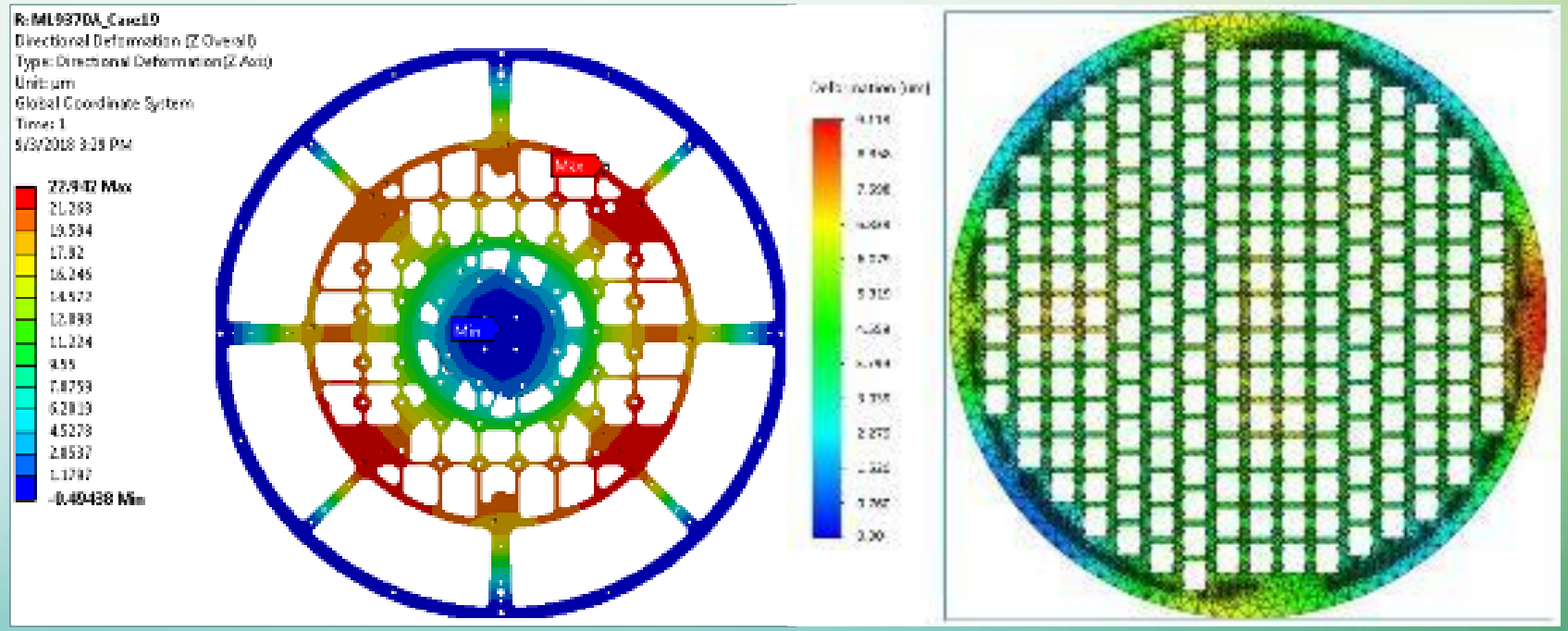


Acceptable SI performance of x32 sharing with TTRE ON

Probe card mechanical strength optimization

- **Mechanical Design:** Achieved <10um contactor deformation for 160,000-probe load condition
- **System stiffness depends on**
  - Probe card weight limitation, test head height and constraint limitation, and available space for electrical components

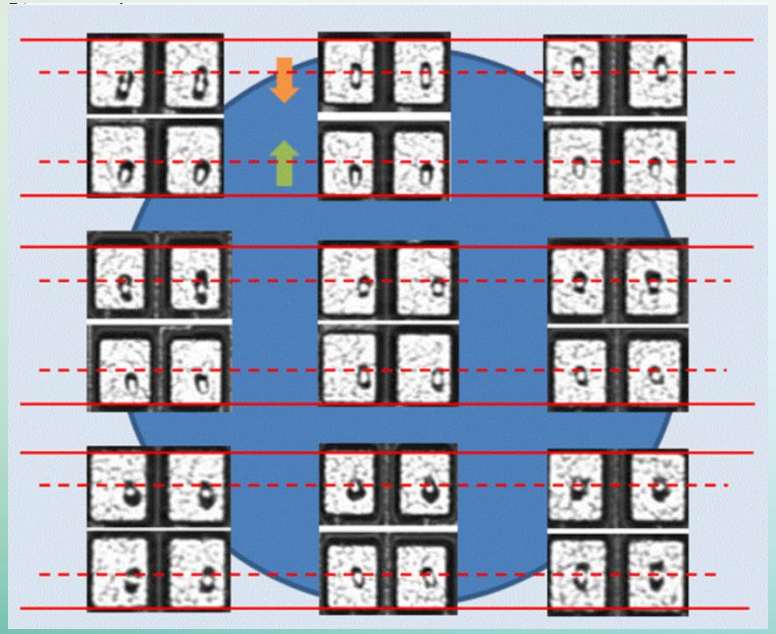
Contactor Deformation [FEA Modeling]	
Overall Deformation	<10um
PC Weight	20Kg
AOT condition	100um



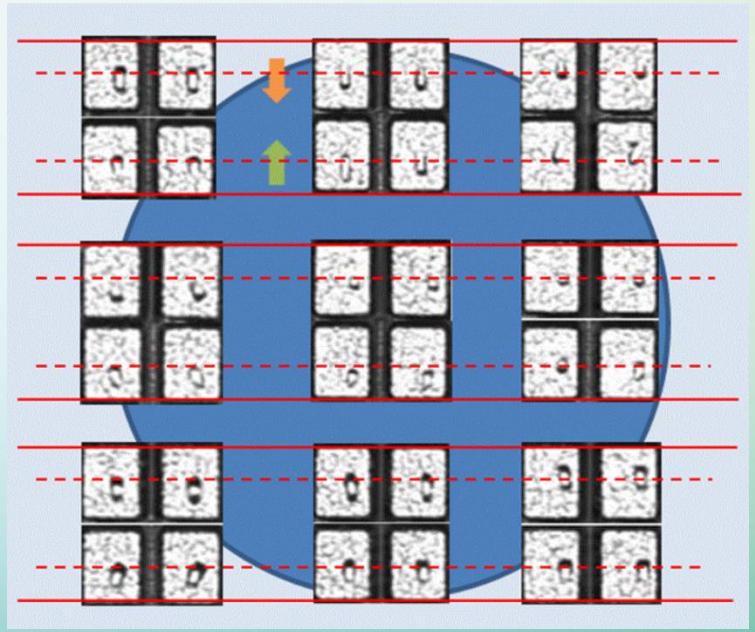
Probe Mark result - Samsung

- **Mechanical Performance:** Stable Contact Resistance achieved for ~160K probes using compact T11 probe at production overtravel
- **Pad Size Capable:** for both hot and cold test condition

Hot Temp Probe Mark



Cold Temp Probe Mark

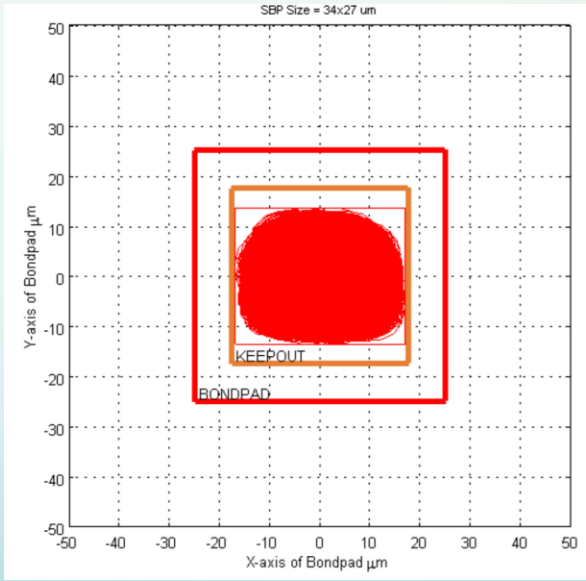


Probe Mark Performance, Touchdown on Pattern Wafer

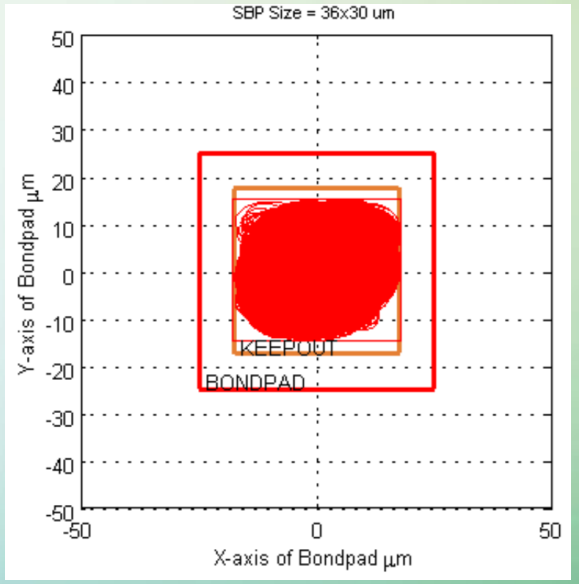
- **Pad Size Capability:** Probe mark keepout performance characterized on pattern wafer to ensure all required operating temperatures are satisfactory

SmartMatrix 3000XP Pad Size Capability	
Pad Size	50um x 50um
Keep out	5um (7um)
High Temp Capability	34um x 27um
Low Temp Capability	36um x 30um

High Temp SBP: 34x27um



Low Temp SBP: 36x30um



Superior probe mark X/Y alignment and Pad Size Capability with 160k probes

SM3000XP Summary

- **Summary**
  - FormFactor and Samsung have collaborated to achieve 1TD production probecard for 3000 DPW device
  - The 1TD SM3000XP probecard enables 50% more wafer throughput versus 2TD probecard alternative. Total wafer test time is decreased by 33%.

- **Acknowledgements**
  - ChangHyun Cho, Samsung EDS Engineer
  - MJ Lee, Cameron Harker, and FormFactor R&D Team

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THANK YOU

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