

A detailed photograph of a microchip probe card assembly. The central focus is a green printed circuit board (PCB) populated with numerous gold-plated micro-bumps. A central gold-colored probe head is mounted on the board, with blue and green wires connected to various points. The background shows the mechanical structure of the probe card, including metal pins and a central cylindrical component. The title 'Chip Scale' is overlaid in large white letters, with a small chip icon above the 'i' in 'Chip'. Below the title, the text 'ChipScaleReview.com' and 'R E V I E W' are visible.

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The International Magazine for the Semiconductor Packaging Industry

Volume 18, Number 1

January • February 2014

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Probing 25 μ m-diameter micro-bumps for Wide-I/O 3D SICs

by Ken Smith [Cascade Microtech] and Erik Jan Marinissen [imec]

Three-dimensional stacked integrated circuits (3D SICs) are emerging as a solution to the speed, power and density requirements demanded by future mobile electronics, as well as high-performance and networking platforms. Through-silicon vias (TSVs) used in 3D SICs shorten interconnects between integrated circuits (ICs), thus reducing power while increasing performance. The electrical inter-die interconnects are typically implemented by means of large-array small-diameter micro-bumps. Wide-I/O DRAM on logic has been identified as a key application for the commercialization of 3D SICs. However, compound product yield conspires to delay full adoption of 3D SICs.

Probe test is essential to improving final stack yield by preemptively identifying the defective devices so they are eliminated before being integrated into otherwise good stacks. Increased test has incremental cost at the die level, but increases yield at final assembly. However, the small dimensions and large array sizes of micro-bumps have made probe test difficult to perform. Researchers at imec have been working in imec's Industrial Affiliation Program on 3D Integration with probe technology partner Cascade Microtech to meet these challenges. They have successfully probed imec test wafers containing a JEDEC Wide-I/O compliant array [1] with 25 μ m-diameter micro-bumps with a high level of accuracy due to the probe-to-pad alignment features of the probe system and the probe card technology used. This article will discuss the large-array, fine-pitch, low-force requirements specific to probing 3D SICs, and detail the methods and tools developed specifically to meet them.

3D SIC assembly test points

Four test points have been identified in the 3D SIC assembly flow. Test point #1 takes place pre-bond, prior to stacking. If the stack consists of three or more die, there is also a mid-bond, partial-stack test. Third is a post-bond test of the completed stack, and lastly is final test performed on the packaged device.

Pre-bond tests may vary in test quality. Virtually all cost modeling exercises agree that some level of pre-bond testing is required to achieve acceptable stack yields. The ultimate in pre-bond testing is known-good die (KGD) testing. KGD testing is a pre-bond test with a quality level equal to final testing, including coverage of at-speed defects and burn-in. KGD testing is especially important when the die or wafers are procured by one manufacturer from another, as the manufacturer procuring the KGDs does not want to pay for bad dies.

Test access for pre-bond testing of the bottom die, as well as mid-bond and post-bond testing of the stack, is through the external I/Os of the bottom die. These I/Os are implemented as large Cu pillars or controlled collapse chip connection (C4) bumps, and therefore probing them is relatively easy. Pre-bond testing of middle and top dies of the stack requires probing on the large-array fine-pitch micro-bumps, and that is where the challenge comes in.

The current workaround

Major semiconductor device manufacturers are already engaged in production of 2.5D and 3D SIC devices, yet they are unable to probe bumps below 50 μ m pitch. They have developed a workaround by using additional, dedicated test pads to facilitate pre-bond testing (Figure 1). Unfortunately, dedicated probe pads come at the expense of increased design effort, more silicon real estate,

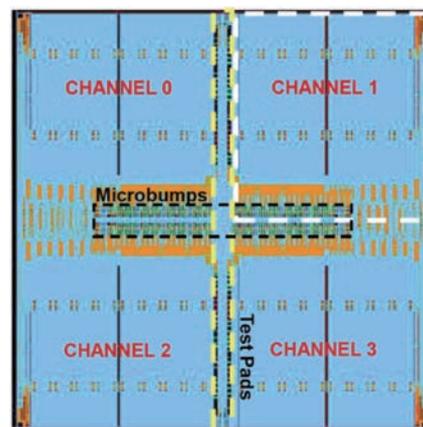


Figure 1: Dedicated test pads are used as a workaround for probing on fine-pitch micro-bumps. SOURCE: Kim et al., Samsung – ISSCC 2011, reprinted courtesy of ISSCC.

additional processing steps and test application time, as well as extra capacitive load on the micro-bump I/O during post-bond functional stack operation. Moreover, testing through dedicated test pads still does not prove the functionality of the micro-bumps themselves. What is best is a solution that allows direct probing on the micro-bumps.

Probe requirements

The target micro-bumps dictate that the metallurgy to be probed is either Cu or Cu (Ni) Sn. For this work, the existing JEDEC Wide-I/O standard of 25 μ m/15 μ m diameter, 40-50 μ m pitch, with an array size of 4x (6 x 50) was used (Figure 2).

Allowable configurations include up to four DRAM “ranks” stacked either on top of the logic die to achieve true 3D, or next to the logic die on an interposer for 2.5D structures. The logic/memory footprint consists of four channels with 300 micro-bumps per channel. Each channel has 128 bi-directional data bits to create the wide I/O, as well as an independent address, control and clock. The interface has shared power and ground.

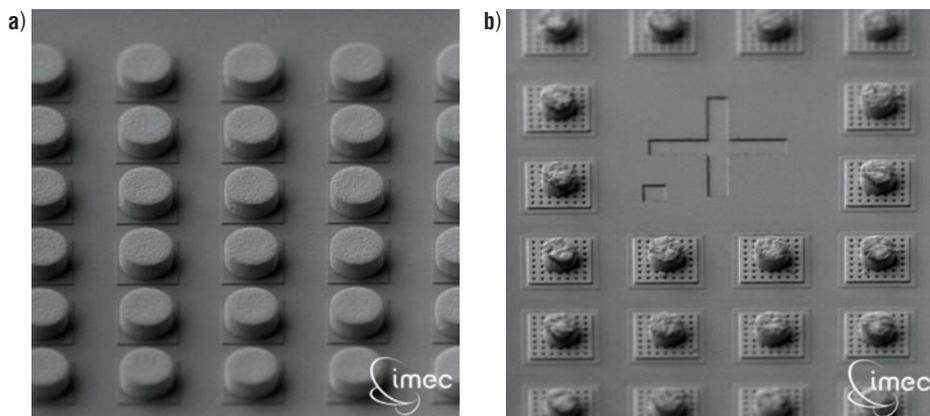


Figure 2: a) (left) 25µm-diameter Cu micro-bumps, and b) (right) 15µm-diameter Cu/Ni/Sn micro-bumps.

To perform the pre-bond test by directly probing micro-bumps, three key requirements have been identified: good electrical contact; limited probe marks; and acceptable cost. Electrical contact calls for low resistance (<5Ω) so as to not impair pre-bond testing of the die. The probe mark profile must be kept under 500nm to keep from impairing downstream bonding. Lastly, the costs of probe cards and stations need to be reasonable.

The right tools for the job

For its development work, imec partnered with Cascade Microtech to evaluate an advanced version of its Pyramid Probe® technology, and performed probe testing on the company’s CM300 probe station, currently installed in imec’s 300mm clean room.

This second generation of the MEMS vertical probe separates the probe tip from the interconnect and puts routing in a separate layer to provide finer pitch and replaceable contacts with more compliance. The probe requires significantly lower force—1g instead of 10g—to achieve adequate contact. Additionally, the probe tip pitch is scalable down to ~20µm (Figure 3).

An accurate probe station is required to ensure that the probe card contactor consistently lands in the right spot. Dual cameras align the wafer with the probe card to achieve the necessary alignment accuracy. The wafer moves in the z-direction and comes in contact with the vertical probe card, which remains stable. As this pre-bond step takes place in the clean room environment, the probe station must be clean room compatible.

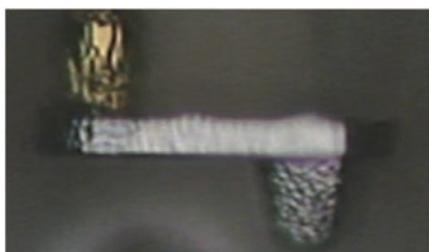


Figure 3: Rocking beam interposer Pyramid Probe®.

Probing 25µm-diameter micro-bumps

The goal of this work was to probe fine-pitch micro-bumps without causing damage, while establishing good electrical contact from the test equipment to the device-under-test, and vice versa.

The wide-I/O probe card touched down on channels A and B to check landing for daisy-chain resistance and probe marks. The aim was to check the influence of probing on stacking. The test demonstrated identical probe marks and a smooth contact resistance profile.

The probe mark consistently measured 6µm, which corresponds to the heel of the diagonally-placed square 6×6 µm² probe tip. From the very shallow probe mark, no negative stacking yield impact is

expected (Figure 4).

Probing 25µm Cu micro-bumps has been successfully achieved, and imec researchers are in the process of probing 15µm Cu Sn-capped micro-bumps, which requires even greater accuracy.

Cost modeling [2] of probing micro-bumps directly versus using dedicated pads indicates that probing on micro-bumps is a lower-cost alternative to testing through dedicated probe pads. The main differentiator is the reduction in test time by avoiding the slow data rates associated with driving data through the reduced set of dedicated test pads, which would make test a significant contributor to the overall cost. Die yield works as a multiplier (at 50% yield, two dies must be tested to find one good one). Comparatively, the cost of probe cards is minor.

Next steps and ongoing work

All the work thus far has been performed on an imec test vehicle dubbed Vesuvius, which was set up for both 3D tests and 2.5D with a passive interposer. The first phase involved interposer wide-I/O probing. The second phase was Vesuvius wide-I/O probing, and the third phase was a 2.5D stack to check daisy-chain bond yield.

While there are four channels to be tested, today the wide-I/O probe card only covers a single-channel (300 micro-bumps) per touch-down (Figure 5). This probe card allows for the study of probe mark impact on the stacking yield, by probing Channels A and B on the (bottom) interposer and Channels B and C on the (top) Vesuvius dies. However, this is in the scope of the experimental test chip only. On a real

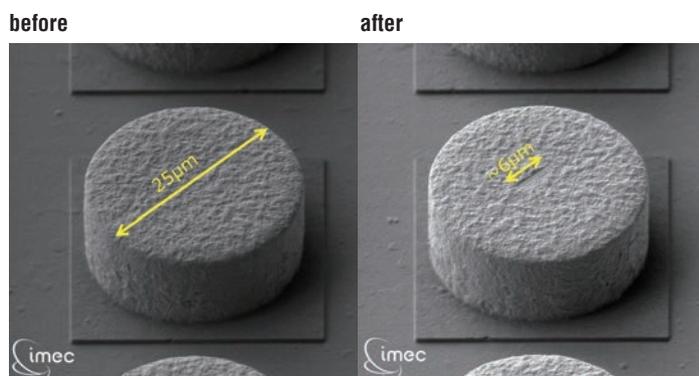


Figure 4: Example of a 25µm-diameter bump before and after probing.

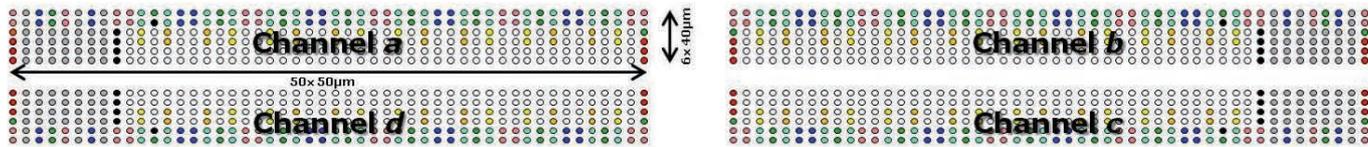


Figure 5: Wide-I/O DRAM interface is laid out in four channels, tested in pairs.

wide-I/O product chip, all four wide-I/O channels would be probed and would require four subsequent touch-downs. Development of a probe core that covers all four channels in a single touch-down is underway.

The drive to finer pitch micro-bumps

Today's micro-bumps come in large arrays at 40-50µm pitch. Pitch is determined by the sum of the bump diameter and the space in between. Typically, bump diameters are 50% or less of the bump pitch. Conventional probe technology can probe 90µm pitch arrays, which have 40-50µm-diameter bumps. They cannot handle 40-50µm pitch bump arrays with bump diameters of 15-25µm. Cascade Microtech's advanced probe technology has been shown capable of successfully probing 25µm-diameter bumps and 40-50µm micro-bump arrays.

In the near future, there will be pressure to further reduce the micro-bump pitch. Although there isn't any JEDEC standard for finer DRAM pitches, logic-to-logic partitioning will assuredly drive the industry to finer pitches. Because 10µm TSV pitches can already be achieved, the burden of increased interconnect density falls to the micro-bumps, and pressure is on to further shrink that pitch to 20µm and even 10µm (Figure 6). Test chips

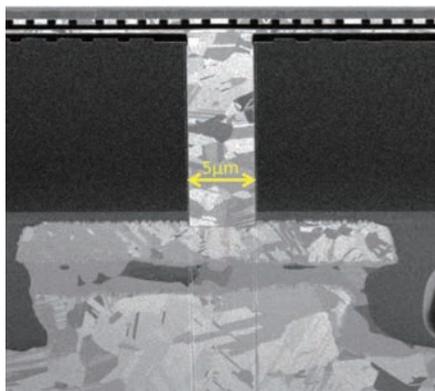
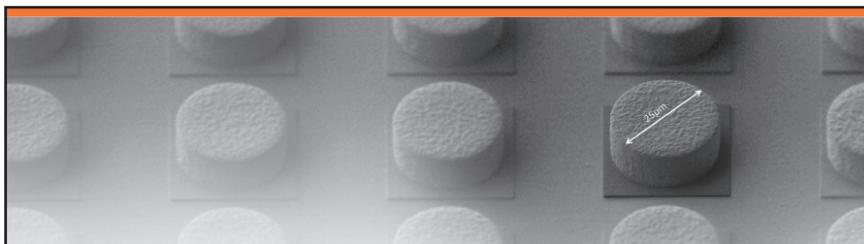


Figure 6: Micro-bumps determine pitch, not TSVs. This SEM photo shows a TSV of 5µm diameter by 25µm height on top of a much larger Cu/Sn micro-bump.

with 20µm-pitch micro-bumps are already available, but it will be an uphill battle to follow the shrinking pitches of the micro-bump roadmap. This push to finer

pitches is putting pressure on probe test methodologies, as well as contactors and equipment suppliers to find solutions that enable fine-pitch, low-force probing.



Accurately Hit 25 µm-diameter Micro-bumps

Breakthrough technology on the CM300 Probe System lets you probe directly on Cu pillar micro-bump wafers, enabling test of 3D-TSV architectures.

The Cascade Microtech CM300, with advanced Pyramid Probe® technology, provides a solution for 3D SiCs that works with "Through Silicon Vias" and allows probing of micro-bumps down to 25 µm-diameter.



Achieve greater probe-to-pad alignment precision and consistent, accurate measurements to increase performance and yield while reducing overall costs. Only Cascade Microtech delivers *reliable light-touch* measurement on delicate micro-bumps.

Find out more about Cascade Microtech's breakthrough technology* at cscd.co/csr-3dtsv

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*Results achieved in collaboration with imec

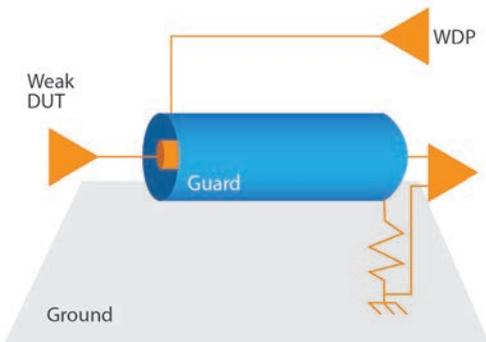


Figure 7: Schematic of the weak driver pre-charge concept.

Work is also underway to address the issue of signal integrity. Three elements to manage this have been identified, including signal routing density, clean power delivery, and weak I/O driver limitations. The wide bus and the I/O are not designed for driving current to automated test equipment (ATE). Weak driver pre-charge (WDP) is a recent breakthrough that involves pre-charging the tester interconnect to a large percentage of the predicted output level. **Figure 7** shows a guarded ground reference for the weak I/O signal lines that is charged by an additional pin driver. The guard is charged in time with the expected output of the weak driver so that there is no voltage differential between the signal and guard, which essentially eliminates the capacitive load of the interconnect. Simulations indicate the expected improvement in rise time and prototype experiments are underway to validate the approach.

Summary

3D SICs are rapidly developing and have attractive benefits. While test challenges remain, work is progressing, particularly in the area of probe technologies and pre-bond test. Direct micro-bump probing is proving to be a more cost-effective and technologically complete method than dedicated pre-bond probe pads. However, it requires advanced probe cards and probe stations. Recent work on test wafers has resulted in successfully probing single-channel wide-I/O micro-bumps at 25µm diameter. Work continues to further prove out this methodology on actual wide-I/O DRAM.

References

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2. M. Taouil, S. Hamdioui, E. J. Marinissen, S. Bhawmik, "Using 3D-COSTAR for 2.5D Test Cost Optimization," IEEE International 3D Systems Integration Conf. (3DIC'13), San Francisco, CA, Oct. 2013.

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