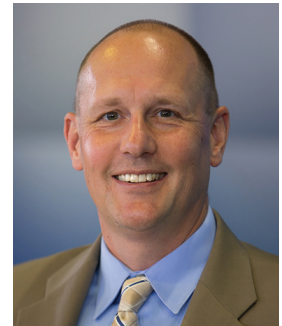


Advanced Packaging, Heterogeneous Integration and Test

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There has been a groundswell of die-integration technologies that are revolutionizing packaging, assembly and test.



THE INTRODUCTION OF AMD'S FIJI CHIP A few years ago marked an important technology turning point for the semiconductor industry. This revolutionary graphics product delivered capability and innovation by relying on the first commercial example of 2.5D heterogeneous integration, featuring a GPU assembled with High-Bandwidth-Memory (HBM) using Through-Silicon-Via (TSV) interconnect and interposer technologies to integrate the various sub-component die. Since then, there have been multiple major products relying on advanced packaging to reach the market; but, perhaps more importantly, there's been a groundswell of die-integration technologies that are revolutionizing packaging, assembly, and test.

What's driving this inflection point? At leading-edge CMOS technology nodes, the benefits of classical Moore's Law scaling are dwindling, and the cost and complexity of achieving that scaling is rising. However, the demand for silicon innovation continues unabated: artificial intelligence, autonomous vehicles, virtual reality, and 5G each demand more intelligence, connectivity, computing power, and speed. For our industry to continue to grow and prosper, the devices used to serve these applications must be more capable, be faster, have a smaller footprint, consume less power, and be more cost-effective, all at the same time.

IDMs, foundries, and OSATs have responded to these challenges with innovative advanced packaging solutions which are a heterogeneous assembly of multiple die in a dense, high-performance architecture that offer more rapidly-customized systems at higher yield. We're still in the early innings of this revolution in integration, and there's a tremendous diversity of enabling solutions for different applications, with no two architectures exactly alike. Here are some examples:

- In Samsung's Aquabolt, which uses the HBM2 (2nd generation high bandwidth memory) architecture, a single 8GB memory chip consists of eight 8Gb HBM2 die, which are vertically interconnected using over 5,000 TSVs per die. It is the industry's first HBM2 to deliver a 2.4 gigabits-per-second (Gbps) data transfer speed per pin [1].
- Intel's Foveros technology is expected to extend die stacking beyond traditional passive interposers and stacked memory to high-performance logic for the first time. The technology provides tremendous flexibility as designers seek to "mix and match" technology IP blocks with various memory and I/O elements to create entirely new products. It will allow these products to be broken up into smaller "chip-lets," where I/O, SRAM and power delivery circuits can be fabricated

in a base die and high-performance logic chiplets are stacked on top [2].

- TSMC's Integrated Fan-Out (InFO) advanced packaging technology was developed for the integration of wireless systems that require low power consumption, good heat dissipation, compact size, and high bandwidths, for applications including smartphone, tablet, and IoTs. This technology has successfully integrated SoCs and DRAM in an advanced mobile application, and is applicable for the 10nm, 7nm, and more advanced nodes [3].

With integration, and consequently value, shifting to packaging and assembly, the role and importance of wafer and die test in the semiconductor manufacturing process is also rapidly transforming. Although there has long been a call from various corners of the industry for Known Good Die (KGD), the test costs to guarantee KGD are not typically a viable economic option. Instead, we need economically feasible strategies to ensure Good Enough Die: strategies that balance cost of test with cost of undetected yield fallout. Of course, in heterogeneous integration, the impact of composite yield fallout due to a single sub-component die does raise the bar on both test coverage and complexity. Chips have to be independently validated at speed before they are stacked or integrated; so,

there is a fundamental requirement for probe solutions to perform electrical test at, or close to, chip operating frequencies. This is compounded by exponentially denser chip layouts and a broad diversity of interconnect/contact materials—from copper TSVs, to solder microbumps. Many advanced applications have two to four times denser contacting patterns than an equivalent monolithic device and probing, therefore, requires driving electrical signals in and out of extremely small structures. This necessitates scalable and cost-effective probe solutions which utilize robotic

but, at the same time, it is important to have enough test coverage to ensure an appropriately low level of sub-component die failures. What is an appropriate level is a question for each individual situation, but it's fundamentally the same question test and product engineers have long faced in the manufacturing of monolithic die.

At this exciting time in the industry, open engagement between customers and suppliers has never been more important for the test community. We must together deploy DFT strategies, decide on where the off-chip test functionality resides,

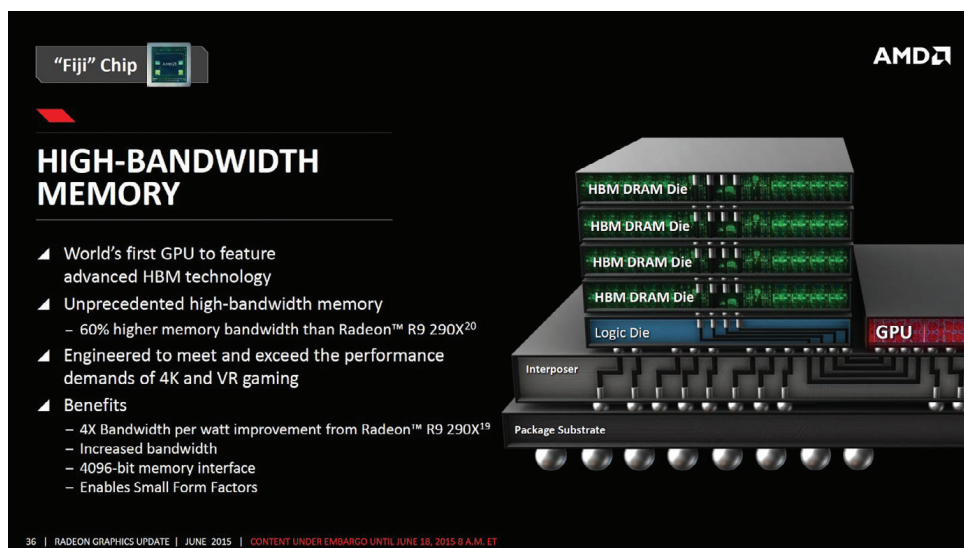


Figure 1. AMD ushers in a new era of PC gaming with world's first graphics family with revolutionary HBM technology.

assembly automation and MEMS to support the competing requirements of fine pitch, high current carrying capability, and lower power impedance. An interesting factoid: a typical MEMS probe is much smaller than diameter of the human hair (100µm), yet carries close to an amp of current at frequencies in excess of 20 gigahertz!

Because the technical and cost challenges for test and probe are so significant, DFT (Design-for-Test) or BIST (Built-in Self-Test) are important tools to help enable economically viable test strategies. Clearly it would be cost-prohibitive and impractical to probe every TSV and micro-bump;

and co-develop comprehensive new test methodologies. We need to work together across all these dimensions to ensure we are not a cost inhibitor for advanced packaging but are, instead, an enabler of the innovative promise offered by heterogenous integration. ³⁶

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