True Kelvin CMOS Test Structure to achieve Accurate and Repeatable DC Wafer-Level Measurements for Device Modelling Applications

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 Agenda

- Challenges for Wafer-Level DC Modeling Measurements
- Typical Probe Contact Resistance vs Scrub Length
- Proposed Test Structure Design
- Experimental Setup
- Characterizing Probe $R_C$ on Test Pads
- Results & Discussions for NMOS measurements
- Recommendations
- Conclusions
Challenges for Wafer-Level DC modeling measurements

- Achieve **Accurate** & **Repeatable** measurements at Different Temperatures
- Reduction in Device Channel Resistance Rds
  - Probe parasitic resistances are Not Negligible!
- Reduction in Pad size (30x30µm to 20x20µm)
  - Smaller tips = large contact resistance
  - Continue using low cost Cantilever probecards requiring longer probe scrub
- How to ensure low Probe $R_C$ at different test temperature?
  - Probe on fresh metallization for 3 times or more on pads ≤ 30x30µm
- Cu Backend Interconnects underneath Al capped pads
  - When exposed, underlying Cu oxidizes rapidly at high temperature
  - Test Wafers goes through thermal cycles, how to repeat the test results 1 year later?
- Wider Thermal test range
  - From -40 to 125 Deg C to -50 to 175 Deg C
Typical Cantilever Probe $R_C$ vs Scrub Length

- > 25µm scrub needed for low probe $R_C$
- Challenging to support 20x20µm pads (Diagonally only 25µm)
  - How to get sufficient scrub, 3 times on the same pad?
Proposed Test Structure Design

- 60nm CMOS devices
- Conventional Test Structure
  - 4 test pads
  - Parasitic Resistances not corrected.
- Probe Kelvin Test Structure
  - 6 test pads
  - Source/Drain with additional Sense (Test Leads and Pads)
  - Parasitic Resistances are corrected.
  - Post layout parasitics simulations
Experimental Setup

- Test Wafer with 60nm CMOS devices
- Cascade Shielded Probe Station
- Keysight Semiconductor Parametric Analyzer B1500
- Single Probe positioner used instead of probe card for test flexibilities
Characterizing Probe $R_C$ on Single Test Pad

- 2 probes on same pad
- 30µm probe scrub
  - Ensure low $R_c$
- 100 contact cycles
  - Re-probing on the same spot
  - Worst-case testing
Characterizing Probe $R_C$ on Single Test Pad

- **25 Deg C Test**
  - 1st 75 Contact Cycles
    - 0.8 to 1 ohms
  - 100th contact cycles
    - 20 ohms

- **150 Deg C Test**
  - Replaced Tips & Check Probe $R_C$ at 25°C
  - 1st 30 Contact Cycles
    - about 5 ohms
  - 43rd contact cycle, underneath Cu oxidizes, resulting in open circuit
Characterizing Probe RC on Test Pads

- Each Probe Parasitic Resistance
  - @ 25 Deg C = 0.4 ohms
  - @ 150 Deg C = 2.5 ohms
- Too large for advanced devices with decreasing Rds.
- Probecard will also have such large parasitic resistance if sense lines are not close enough to the device terminals.
Results & Discussions for NMOS Measurements
Id & Rds vs Vd @ Vg=1.2V, 25°C, 100 contact cycles for 60nm NMOS

- Kelvin Test structure
  - Accurate and very repeatable results over 100 Contact Cycles
  - Probe parasitics are corrected
  - Larger Id & Smaller Rds

### Conventional Test Structure vs Proposed Kelvin Test Structure

- **Large Deviation**
- **Vd=0.6V & 1.2V**
- **High Repeatability**
- **Vd=0.05V**

- **Id**
  - Large Deviation
  - 49-58mA

- **Rds**
  - Large Deviation
  - 20.8-24.6Ω

- **Id vs Vd**
  - Large Deviation
  - 64mA

- **Rds vs Vd**
  - Large Deviation
  - 18.8Ω
Id & Rds vs 100 Contact Cycles @ 25°C for 60nm NMOS

- Kelvin vs Conventional Test Structure
  - Measured Id & Rds is extremely stable & repeatable throughout 100 contact cycles.
  - Sense line of B1500 is able to correct and mitigate the increase in Rc.
  - Probe tip cleaning not required.
Characterizing Probe $R_C$ on Single Test Pad

![Graph showing the increase in $R_C$ over contact cycles.](image)

- **Series Resistance (ohms)**
  - Scale: 1.0E-01 to 1.0E+12
  - Logarithmic scale

- **Number of Contact Cycles**
  - Range: 0 to 100

- **Conditions**
  - 25 Deg C (Blue line)
  - 150 Deg C (Red line)

_**Increase in $R_C$**_
● Kelvin Structure
  – 1\textsuperscript{st} Contact Cycle, $I_d$ larger by 30%, $R_{ds}$ much smaller
  – 43\textsuperscript{rd} Contact Cycle, failure due to underlying Pad Cu fully oxidized
Characterizing Probe $R_C$ on Single Test Pad

![Graph showing series resistance vs. number of contact cycles for 25 Deg C and 150 Deg C. The graph indicates a failure point.]
Recommendations

- **Recommended Test Sequence:**
  - Hot Temp ⇒ Room Temp ⇒ Cold Test
  - Test Structures are not probed yet, minimize exposed Cu oxidation
- **Adopt an Inert Test Environment**
- **Adopt Thicker Al. top cap layer**
- **Adopt Larger Pad (Fresh Metallization)**
- **Invest in Vertical Probe Card with frequent Tip Cleaning Cycles**
  - Possible to minimize probe parasitics
  - Test Leads not corrected, affects Model accuracy
- **Invest in True Kelvin Probe Tips**
  - Bigger or Longer pads to accommodate 2 Tips
  - Test Leads not corrected, affects Model accuracy
- **Adopt True Kelvin Test structure**
Conclusions – Adopt True Kelvin Test Structure as it…

- Corrects Probe parasitic resistances (Vary with Temperature).
- Corrects Test Leads parasitic resistances
  - Models should not account for test leads).
- Minimizes Retest & Revalidation
- Allows repeated probing of Same Device without Accuracy Degradation.
  - Example: Retesting of Golden Wafer for Model development after 1 year of model release
- Allows handling of small test pads < 30x30µm with cantilever probecard
  - Using smaller probe scrub and smaller probe tips
- No Probe Tip Cleaning required!
  - if B1500 has sufficient voltage headroom to correct for Parasitic Resistances.
- Mitigates $\uparrow R_C$ due to oxidation of underlying Cu underneath test pads.
- Though larger layout, provides Accurate Results with Lower Cost of Test
Thank You!
Questions?