Wafer-level Electromigration for Reliability Monitoring

Quick-turn Electromigration Stress with Correlation to Package-level Stress

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***Abstract*— Rapid, accurate and flexible reliability characterization capabilities are important tools in process development and monitoring. Electromigration evaluation has largely relied on packaged test structures given the need for high temperatures to provide sufficient acceleration. However, several Wafer-Level (WL) electromigration (EM) techniques and their correlation to Package-Level (PL) tests have been reported (e.g. SWEAT[1],[2] , isothermal[3], tests). Presented in the this paper is a wafer-level electromigration test that addresses the PL correlation issues presented by quick-turn tests, but maintains the advantages of wafer-level and allows quick comparison to PL baseline with a significant advantage in time-to-data over PL-EM testing. Statistical matching of initial resistance (R0) and Time-to-Failure (TTF) between PL vs. WL electromigration tests on two concurrently stressed structures across sixteen reticle locations is demonstrated. This WL-EM stress technique provides equivalent TTF, with no reliance on extrapolations, whilst yielding an advantage in time-to-data relative to standard PL-EM tests.**

Keywords-Wafer-leve; electromigration; SWEAT; isothermal; package-level

I. INTRODUCTION

The continued aggressive scale reduction and application of novel alloys to metal interconnects in semiconductor manufacturing processes presents increasing concerns over issues of reliability. This increased risk, coupled with the seemingly constant acceleration in the cadence of process development requires not only reliable and accurate reliability data, but expeditious reliability data generation. Electromigration (EM), being one of the primary reliability concerns, testing is customarily performed to determine metallization lifetime using constant current, package-level (PL) EM tests.

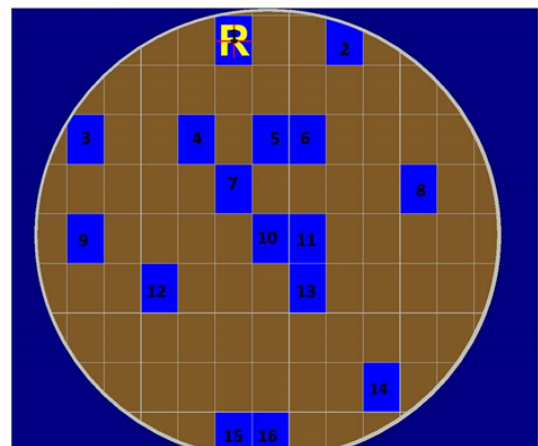

Figure 1. Reticle locations with site numbering accessed by multi-site probe card (300mm wafer).

The advantages of PL-EM tests lie in their cost efficiency, accurate temperature control, and creation of results that can be extrapolated to use condition through the application of Black's law in a fairly straight-forward manner and without the empirical assumptions in methods such as in Standard Wafer-level Electromigration Accelerated Test (SWEAT) [1] or Isothermal tests [2].

Package-level tests require the substrate on which the test structure is manufactured, to be sawn in the presence of water and then die-attached to a suitable integrated circuit (IC) package. This exposure to water and subsequent thermal cycling in die attachment presents risk to the integrity of the test structure (especially in the absence of a hermetic guard-ring), which may lead to artifacts in PL-EM test results. The die is then wire-bonded to the lead-frame of this IC package to allow ohmic contact to the anode and cathode of the test structure.

Not only does this process present risks to the test structure through oxidation and possible exposure to ESD events, it also takes time (approximately one week) that might be better spent running another test. For stress biases resulting in a full distribution of failures in one week, packaging of the test structure effectively doubles the time-to-data (TTD).

This added time budget presents a problem when quick results are required, such as in production monitoring where one might want to determine the impact to EM lifetime of an excursion in the process. Further, with the increased cadence of process development, quick-turn electromigration data is desirable to inform manufacturing process decisions (e.g. design rule, material selection, process integration).

Much work has been done to enable quick and reliable EM testing. Work has been centered on highly accelerated wafer-level (WL) electromigration testing methods (e.g. SWEAT[1], isothermal[2]), thereby obviating the need for package assembly of the test vehicles. Not only do these methods save a week by not requiring IC packaging, their test durations are on the order of thousands of seconds, as opposed to tens-to-hundreds of thousands of seconds for PL-EM.

Although correlation has been shown to package-level result [3], [4], there still exists uncertainty regarding equivalent failure mechanisms between SWEAT and isothermal tests, and standard constant-current PL-EM tests. Further, such highly accelerated WL-EM methods require fairly complicated testing algorithms, a priori knowledge about the degradation behavior of the structure, specially designed test vehicles[5], or assumptions about the joule heating of the structure as it degrades. (e.g. targeting of time-to-fail by varying current in SWEAT method or use of joule-heating to lower the activation energy of the failure mechanism).

SWEAT and isothermal tests also present a problem when the semiconductor process is changed dramatically (as is often done during the research phase of process development) as WL to PL correlations developed through the comparison of baseline processes, can be specious [6].

In the following we present a WL-EM test method that does not require high-acceleration, but addresses some of the concerns regarding time-to-data (TTD). Unlike highly accelerated WL tests, we do not rely on joule-heating of the test structure to lower the activation energy, but instead utilize a heated chuck. The tests are performed using constant current-stress; identical to PL-EM method to avoid questions regarding failure kinetics and mechanism.

II. EXPERIMENTAL

A. Test System

A Cascade Microtech Inc. (CMI) El;ite 300 prober was modified with a 350C thermal chuck, nitrogen purged probing environment with oxygen sensor, full-travel bridge camera, and mounting for a multi-site probe card centered on the chuck.

The Celadon Inc. probe card was comprised of a 320mm, low coefficient-of-thermal-expansion (CTE) alloy plate machined with 16 randomly placed recesses [Fig. 1]; spaced between centers to match integer multiples of the reticle-to-reticle dimensions of the wafer patterning. A ceramic button containing a 2X6 row of probes with pitch equivalent to test row pad pitch was bonded into each of the sixteen sites. Borosilicated glass windows were then bonded on top of these buttons, allowing visualization of probe contact of all sites whilst maintaining the inert environment of the probing environment. This probe card allows contact to sixteen pad rows simultaneously as the chuck is raised.

The probe card was attached, via cabling to a CMI reliability testsystem, allowing concurrent EM testing of two structures per pad row, simultaneously.

B. Test Structures

Two standard dual-damascene structures were selected for testing: V3M3 and V3M4 [Fig. 2] structures, manufactured on Intel Corporations 14nm process. The V3M4 structure was standard via/metal "down-current" structure whilst the V3M3 was an "up-current" one, both representing nominal process conditions and were selected due to the quality of the extant baseline data for these metal layers previously collected utilizing PL-EM tests.

Wafers were patterned with multiple via links to large (~200X200µm), Ti coated pads in a 2X6 pattern. The pad size was designed to provide margin against thermal expansion.

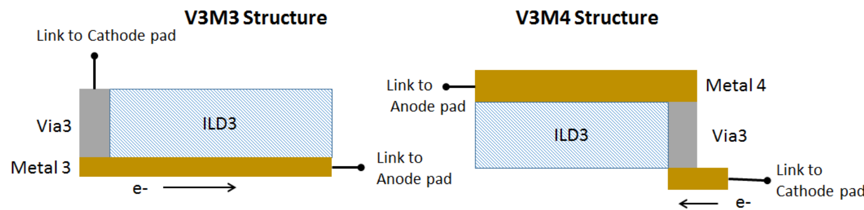

Figure 2. Test structure geometry and current flow

C. *Test Execution*

Two wafers were prepared for our first round of tests from two separate fab lots. Wafer 1 and 2 were individually stressed at 300C with current densities that would yield small self-heat values with respect to stress temperature. Since the system is capable of providing different stress currents to more than one structure independently, during each wafer run, both structures were tested simultaneously. Time to failure (TTF) is regarded as 10% resistance increase of initial resistance (R0), measured at 300 C. Resistance data is collected in-situ stress, at a time interval of seconds.

After both wafers were tested on the WL-EM system, they were diced and packaged for PL-EM testing. Each structure was packaged individually, so that although both the V3M3 and V3M4 structures tested at WL were of the same reticle location, their PL controls were from separate reticle locations, each offset one reticle from the WL tested reticle. Both WL-EM and PL-EM had 16 devices under test for a given distribution. The packaged structures were tested in a PL-EM stress system under equivalent conditions to those applied at WL.

III. RESULTS

The distributions of (TTF) of each structure tested in the WL-EM system were compared against those generated by the PL-EM system, by using a typical Wilcoxon Group Homogeneity test. Figure 3 shows the results for the “current up” structure V3M3 and Figure 4 shows the results for “current down” structure V3M4 on Wafer 1. For both cases, a relatively low Chi-square value (<10) and large Prob>ChiSq value (>0.05) is observed. This indicates that the difference between PLEM and WLEM TTF distributions are statistically insignificant.

R0 distributions were also compared between equivalent structures from the same wafer tested by both methods. A two-tailed t-test of means assuming unequal variances was performed on each pair of distributions and a p-value >0.05 was regarded as demonstrating equivalence.

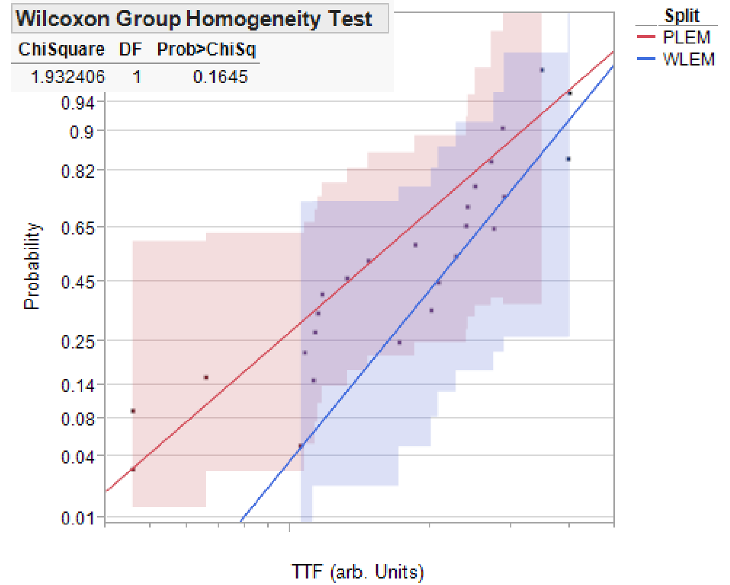

Figure 3. Cumulative probability plot overlays of TTF for PL vs. WL for V3M3 structure on wafer 1 and Wilcoxon test result.

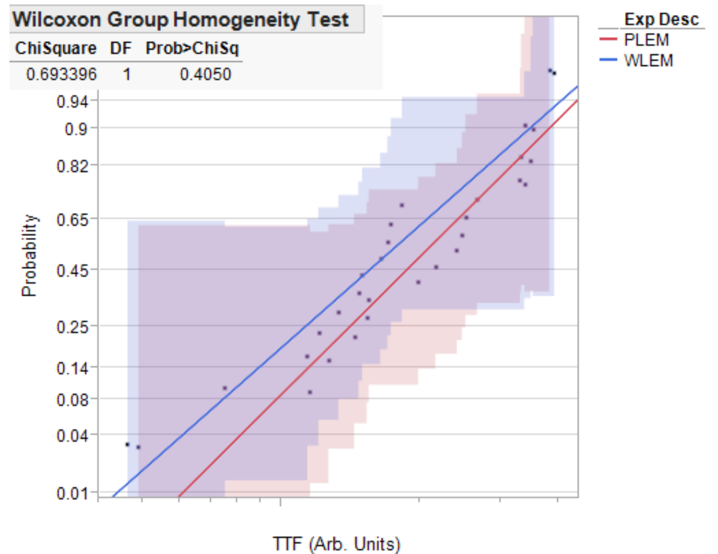

Figure 4. Cumulative probability plot overlays of TTF for PL vs. WL for V3M4 structure on wafer 1 and Wilcoxon test result.

Five sites had to be excluded for high contact resistance during the WL tests on wafer 1. This issue with contact resistance (Cres) was also seen in the R0 data where the WL

tests shows higher resistance for non-excluded devices under test (DUT's) compared to PL test yielding a p-value of 0.999 for WL R0> PL R0 on the V3M3 [Fig. 5] structure and 1.000 for the V3M4 [Fig. 6]. As these are not full Kelvin structures; a serial Cres will not only show up in R0, but will show up in TTF as it affects the percent resistance change necessary to terminate stress of a structure. This TTF artifact will be most apparent on lower resistance structure w.r.t. Cres as Cres will represent a higher percentage of the R0 measurement.

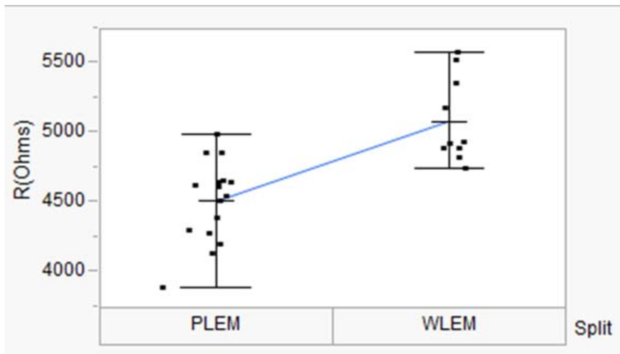

Figure 5. Comparison of R0 distributions for PL vs. WL for V3M3 structure from wafer 1.

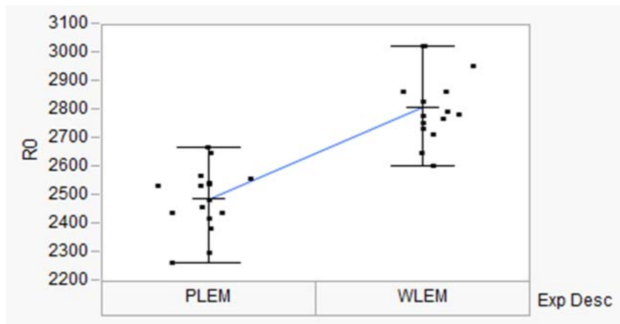

Figure 6. Comparison of R0 distributions for PL vs. WL for V3M4 structure from wafer1

Better protocols for initial planarization of the probe card plate w.r.t the chuck yielded better results on subsequent tests which yielded good contact on all 16 sites. This planarity issue developed over multiple thermal cycles of the probe card and was due to the plate warping. After the probes were realigned to compensate, good contact was demonstrated on all but site 2, which was found to have a broken sense line [Fig.7]. Design changes to the probe card plate have been applied to address warping issues; and as of time of publication are not yet rigorously tested.

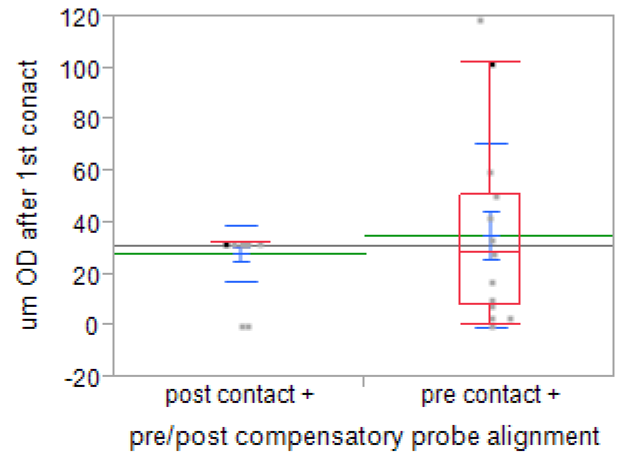

Figure 7: Comparison of chuck height (μm) to contact, past first site contact for all probe rows, pre vs. post compensatory alignment. Chuck height +/- 10μm.

The distributions of TTF on wafer 2 shows a similar trend to that of wafer 1. Figure 8 shows the results for the "current up" structure V3M3 and Figure 9 shows the results for "current down" structure V3M4 on Wafer 2. The relatively low Chi-square value (<10) and large Prob>ChiSq value (>0.05) again indicate that the difference between PL-EM and WL-EM TTF distributions to be statistically insignificant. R0 distributions for both structures across test methods show equivalence, yielding a p-value of 0.2 and 0.25 for the V3M3 and V4M4 structures respectively [Fig. 10,11].

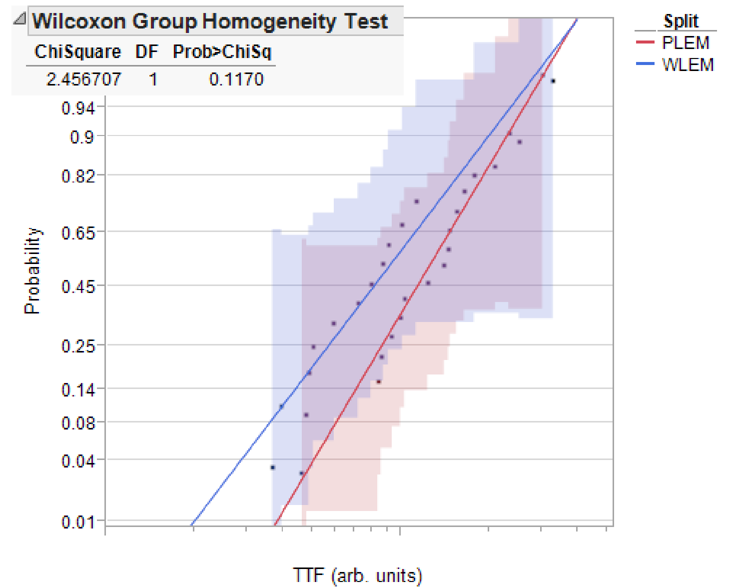

Figure 8. Cumulative probability plot overlays of TTF for PL vs. WL for V3M3 structure from wafer 2 and Wilcoxon test result.

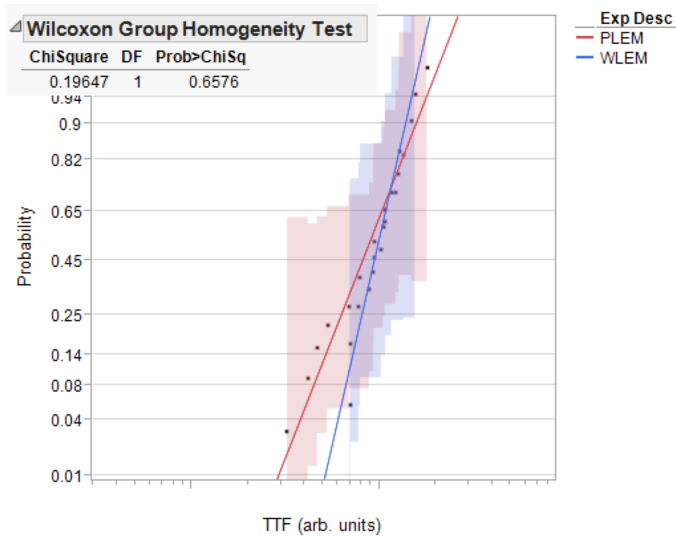

Figure 9. Cumulative probability plot overlays of TTF for PL vs. WL for V3M4 structure from wafer 2 and Wilcoxon test result.

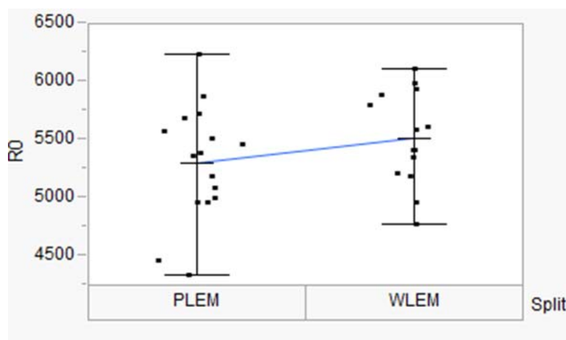

Figure 10. Comparison of R0 distributions for PL vs. WL for V3M3 structure from wafer 2

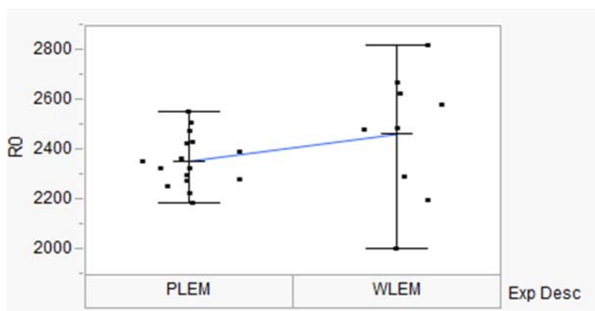

Figure 11. Comparison of R0 distributions for PL vs. WL for V3M4 structure

IV. CONCLUSION

A wafer-level alternative to conventional package level EM testing is demonstrated and a comparison of electrical data is established. Wilcoxon Group Homogeneity tests on TTF distributions show clear sign of statistical equivalence. Results from two structures (current up and current down) in two wafers, show that four instances of TTF distributions for WL-EM to PL-EM data indicating that they are not statistically different from each other. Clearly much work remains to be done to demonstrate equivalence of these package-level and wafer-level constant current EM testing techniques. Most of these issues, including the planarization issue observed with wafer 1 but fixed for wafer 2, appear to be instrumental complications that can be fixed with incremental changes to the system.

We believe the advantage in time-to-data provided by this wafer-level electromigration system as well as the decreased risks of packaging related artifacts, decreased risk for electrostatic discharge, and the non-destructive nature of the test that leaves the entire wafer unsawn, makes it a valuable compliment to standard package-level testing and a viable “quicker-turn” electromigration stress technique. Development of this technique in the long run could be very beneficial to those testing reliability of metals under accelerated stress conditions.

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