FormFactor™

Leveraging Semiconductor Fabrication Processes and High-Volume Test to Advance Quantum Technologies



Beverly Boiko

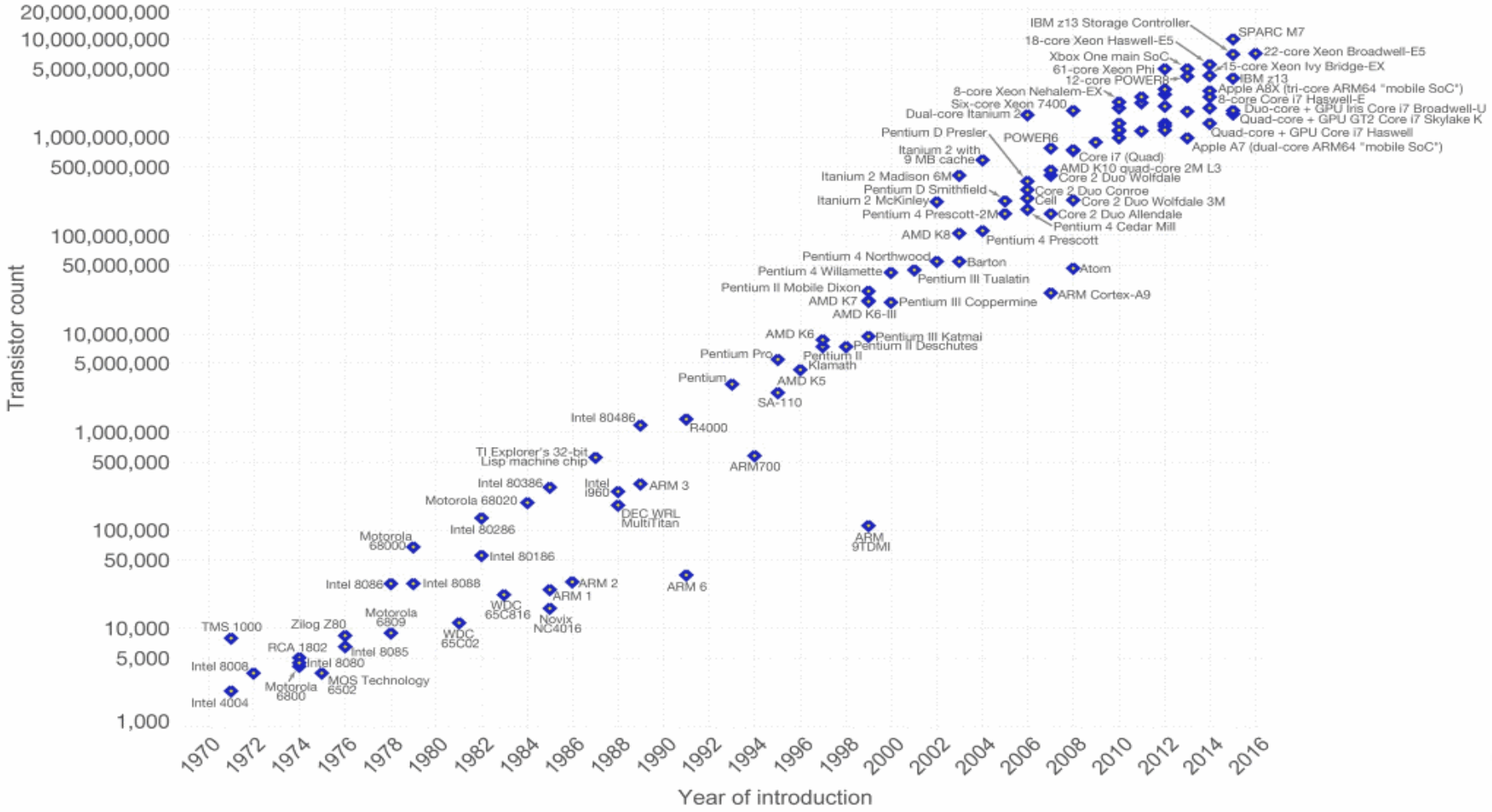
Sr. Principal Applications Engineer



Moore's Law – The number of transistors on integrated circuit chips (1971-2016)

Our World in Data

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.

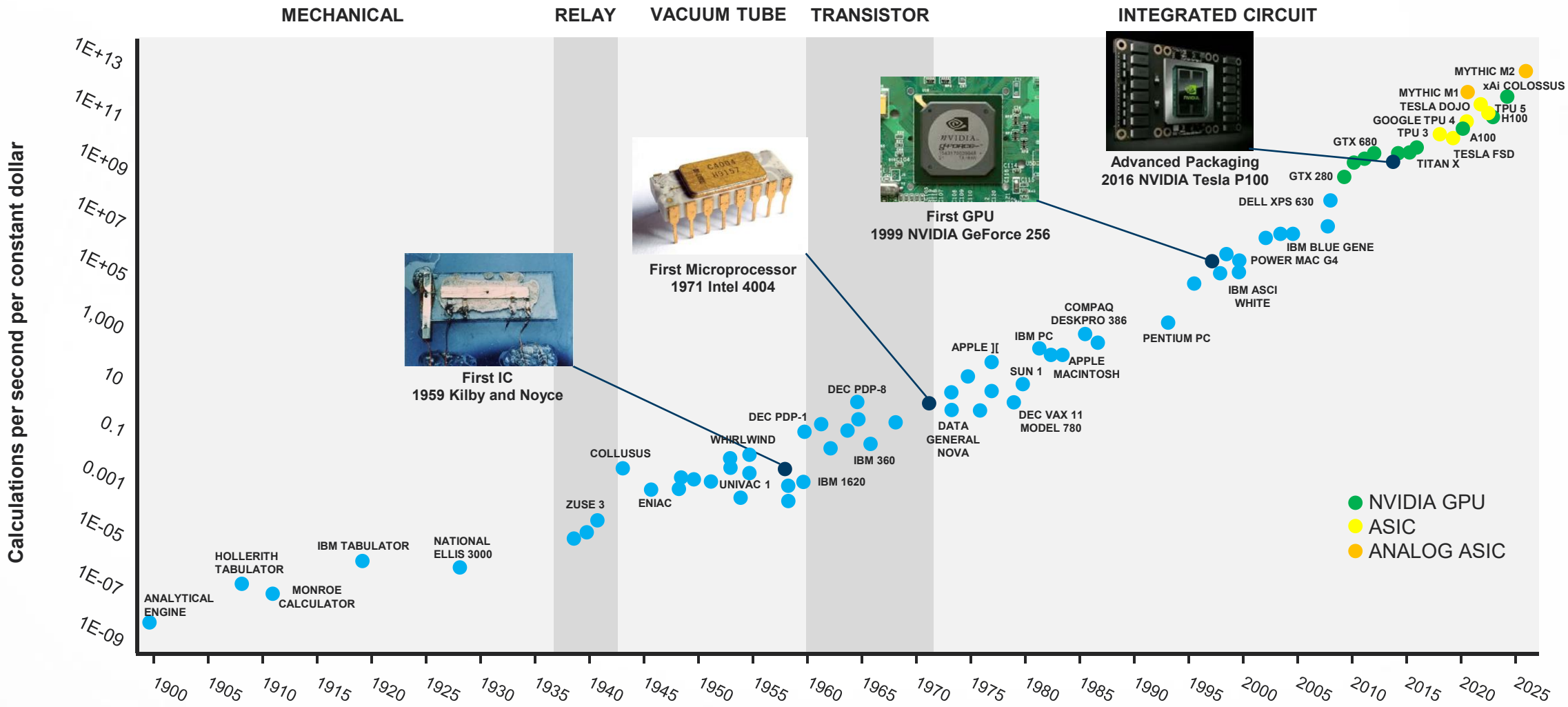


Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Licensed under CC-BY-SA by the author Max Roser.

FormFactor™

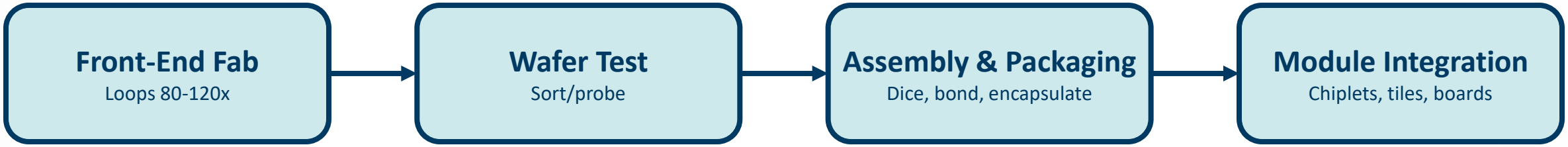
128 Years of Moore's Law



Source: Ray Kurzweil, updated since 2008 by Steve Jurvetson, Future Ventures

FormFactor™

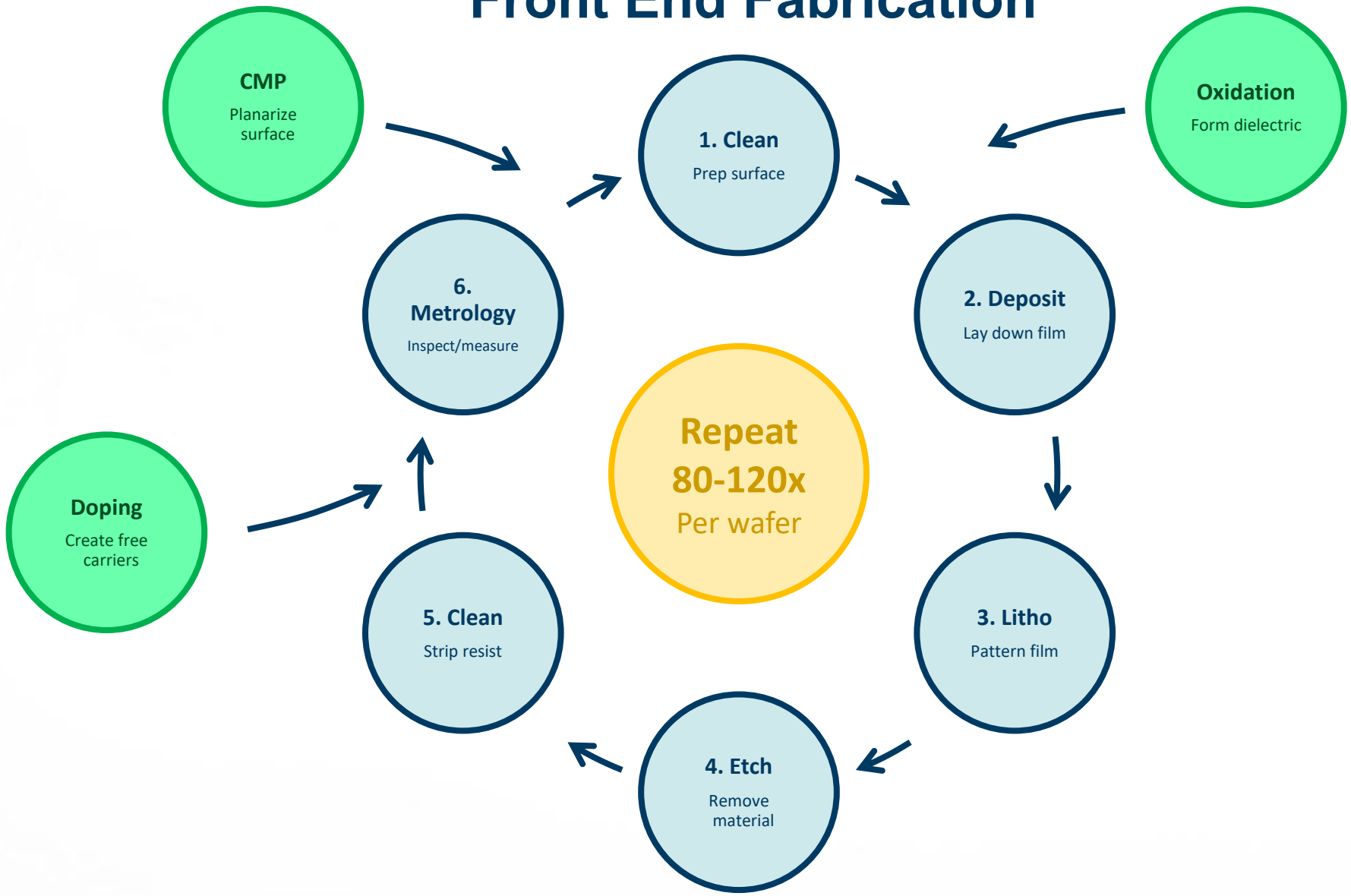
Semiconductor Manufacturing



https://semiconductorx.com/semiconductor-manufacturing-steps.php

FormFactor™

Front End Fabrication



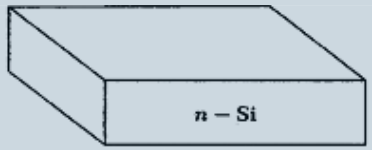
https://semiconductorx.com/semiconductor-manufacturing-steps.php

FormFactor™

Unit Processes

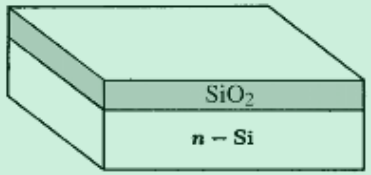
Clean

1)



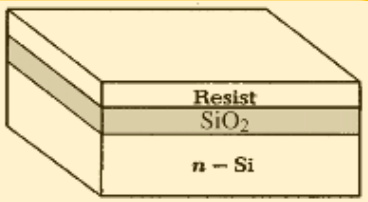
Oxidation

2)

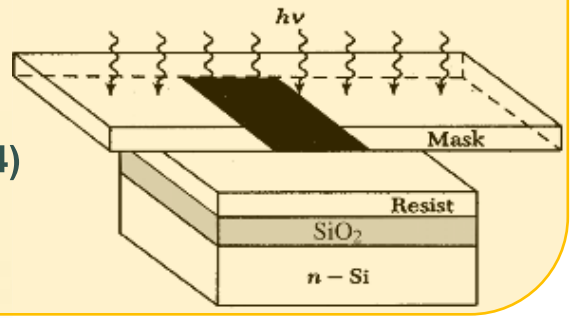


Lithography

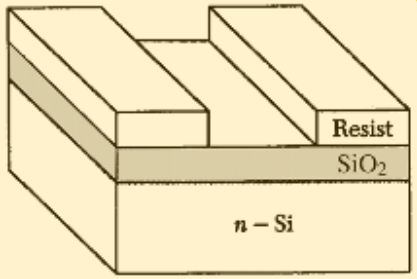
3)



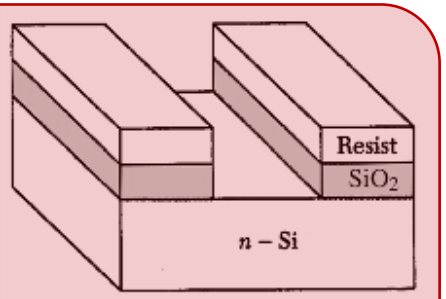
4)



5)

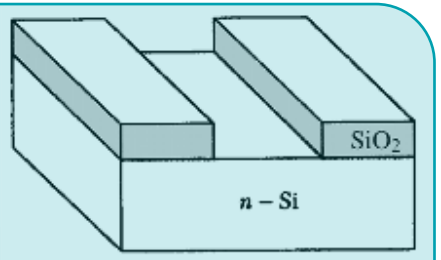


6)



Etch

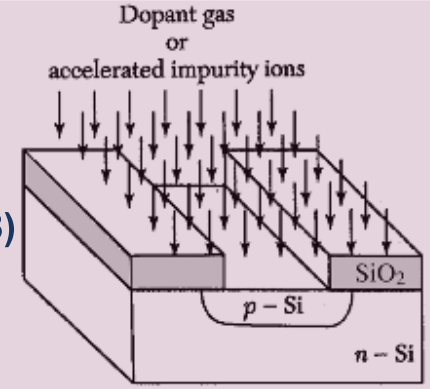
7)



Strip

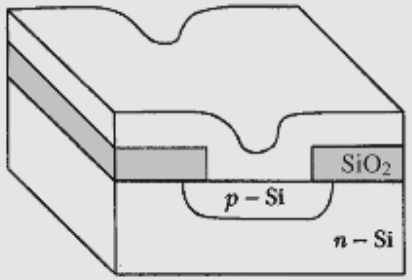
Doping

8)

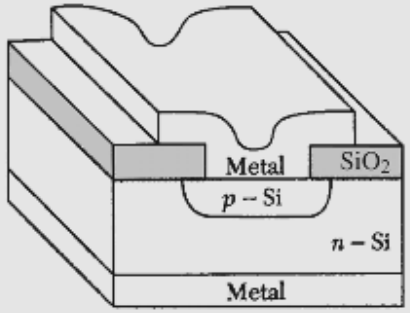


Metallization

9)



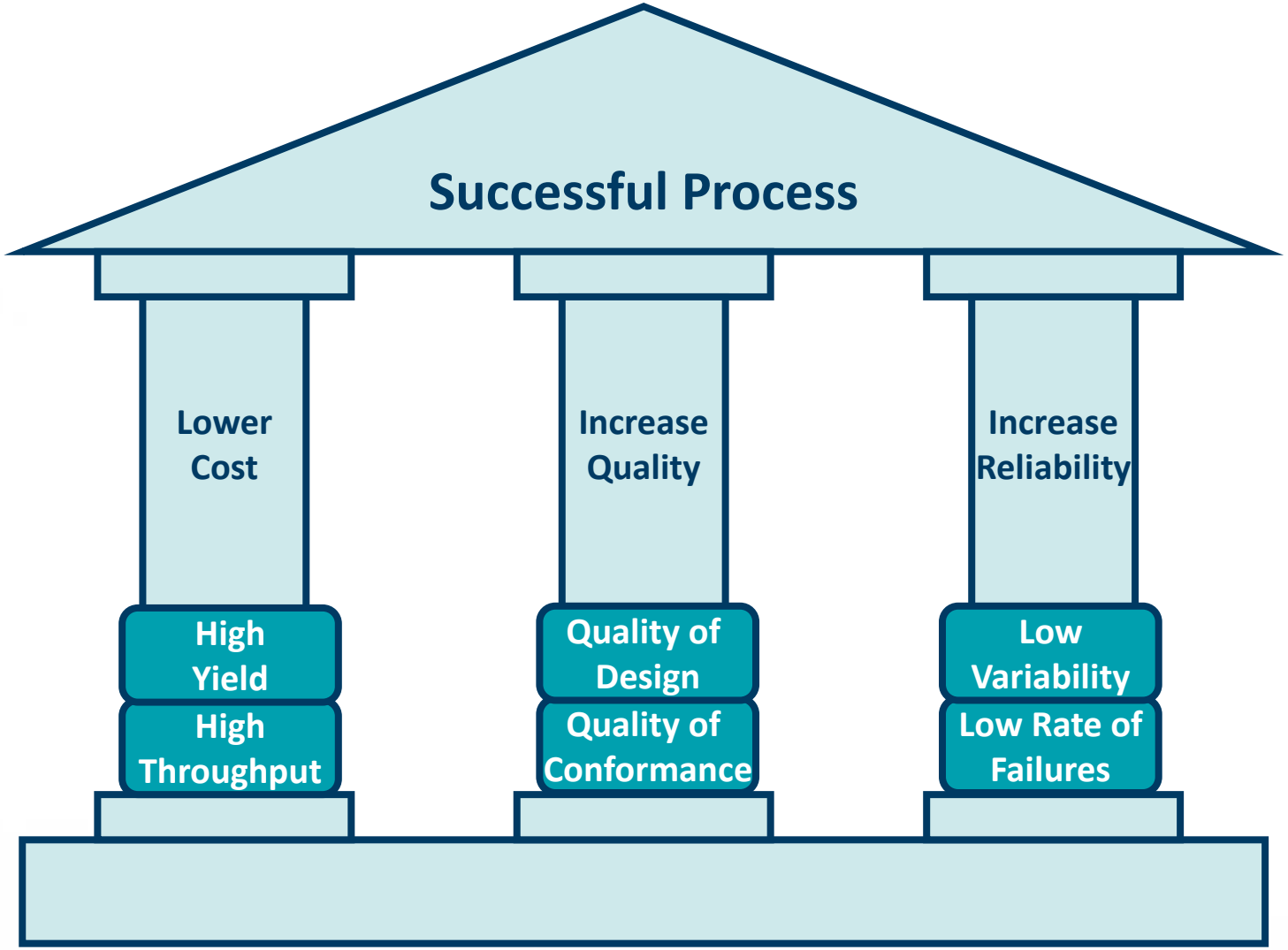
10)



May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

FormFactor™

Goals of Semiconductor Manufacturing

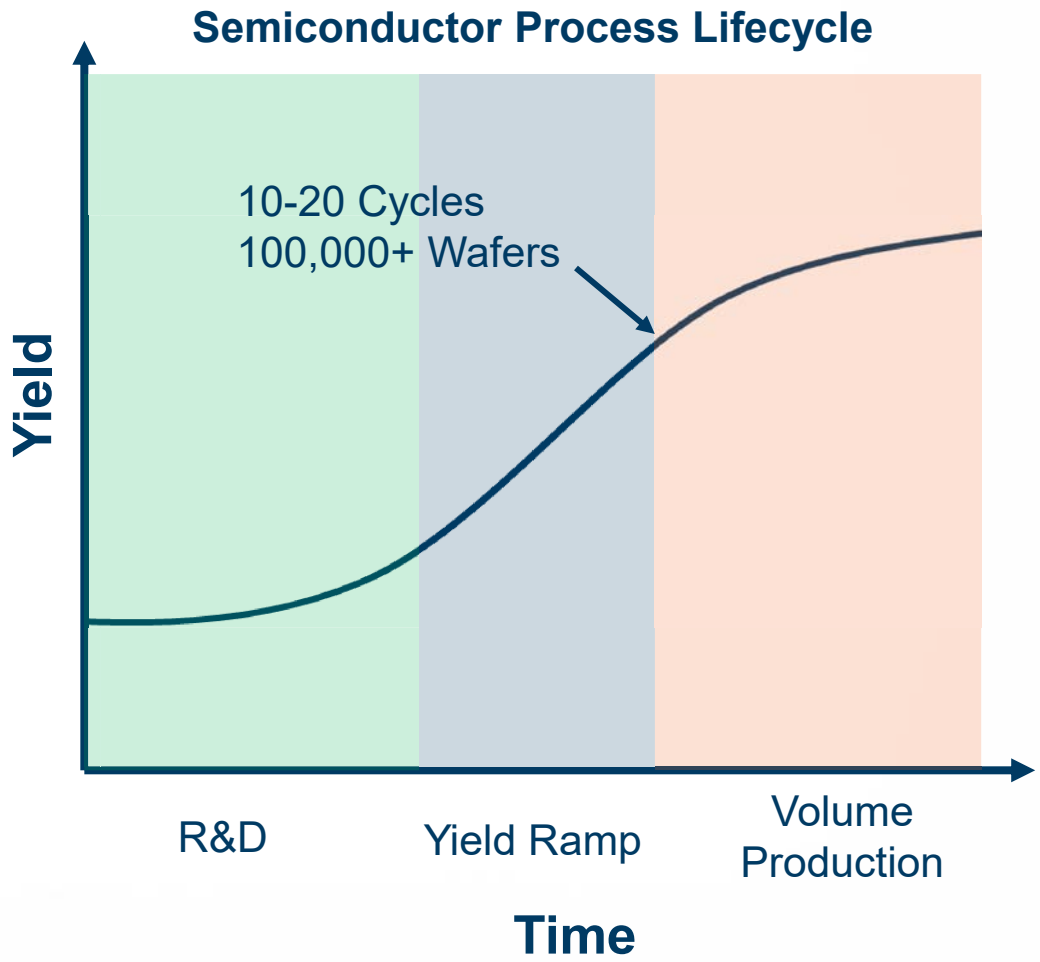


May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

FormFactor™

Yield Learning Cycle



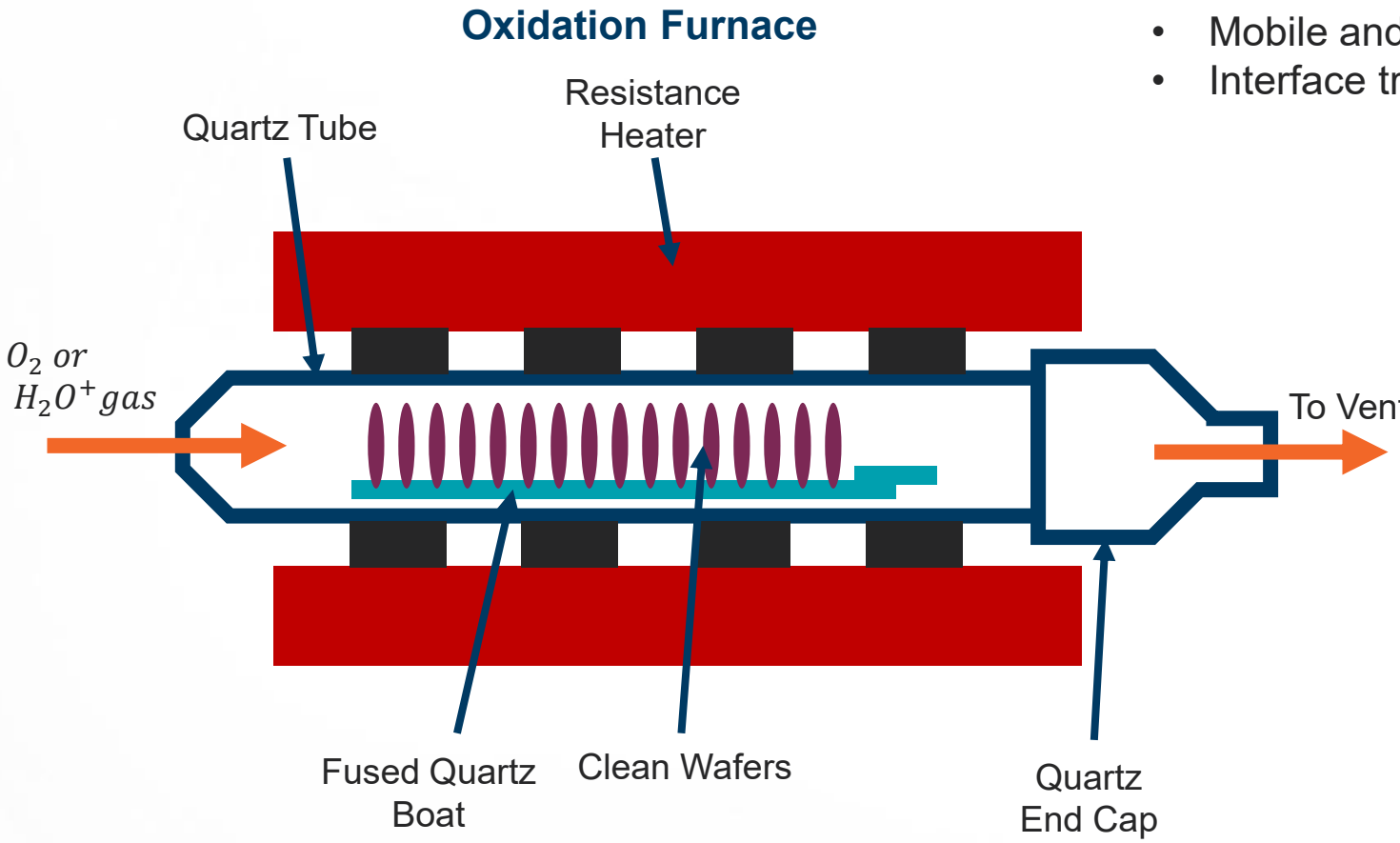


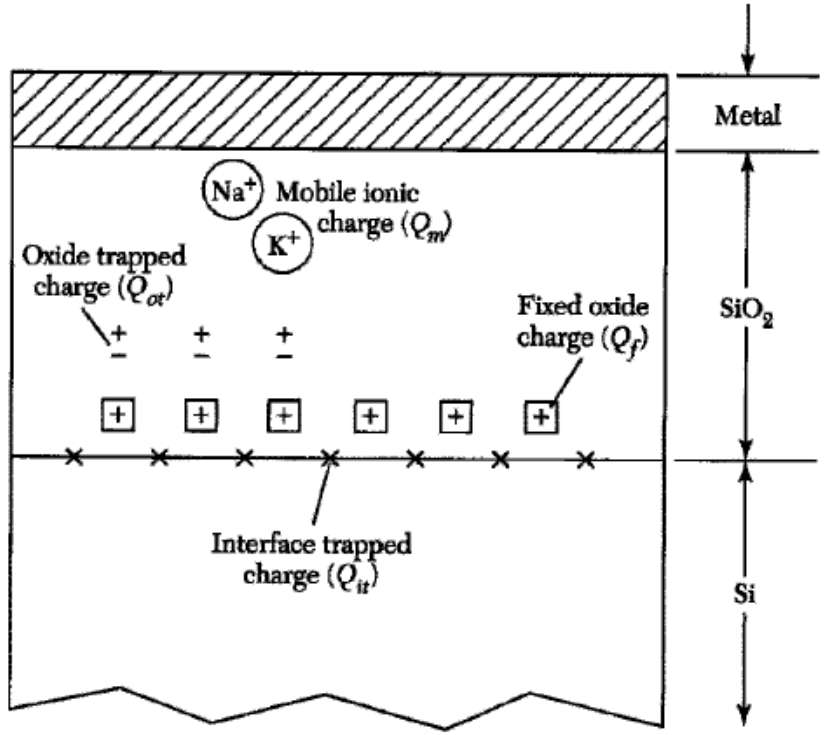
Weber, C. (2004). Yield learning and the sources of profitability in semiconductor manufacturing and process development. *IEEE Transactions on Semiconductor Manufacturing, 17*(4), 590–596.

FormFactor™

Fab Challenges: Oxidation

- Oxide thickness must be tightly controlled
- Mobile and trapped charges can alter the threshold voltage
- Interface traps can be a source of noise



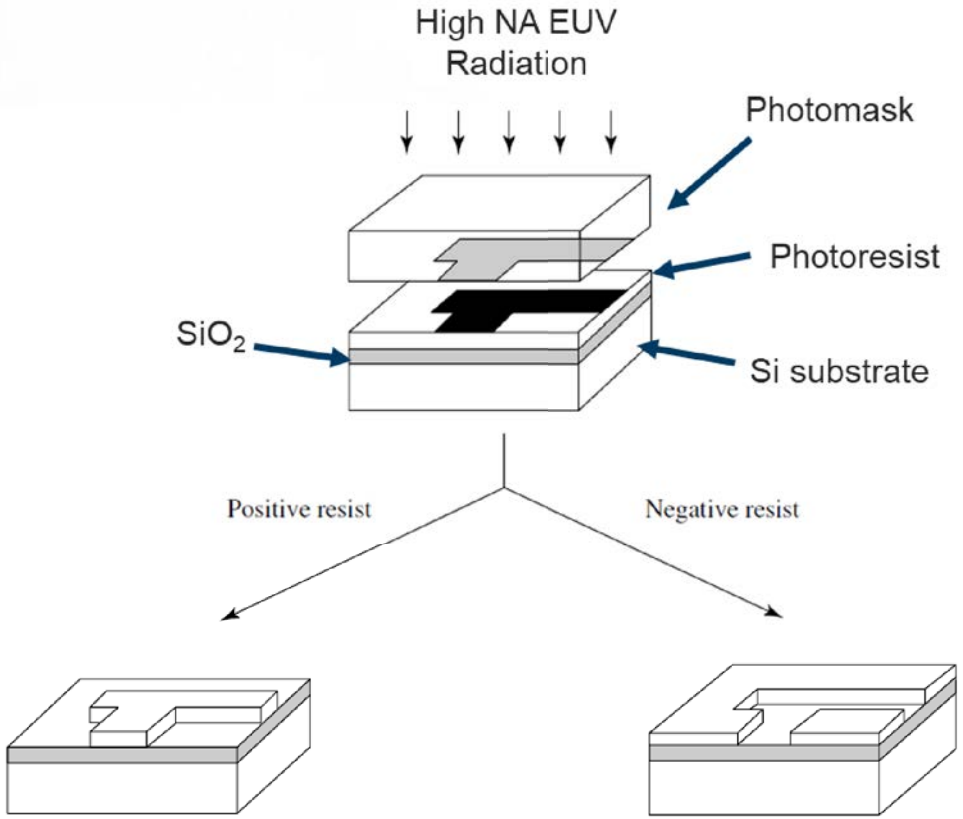


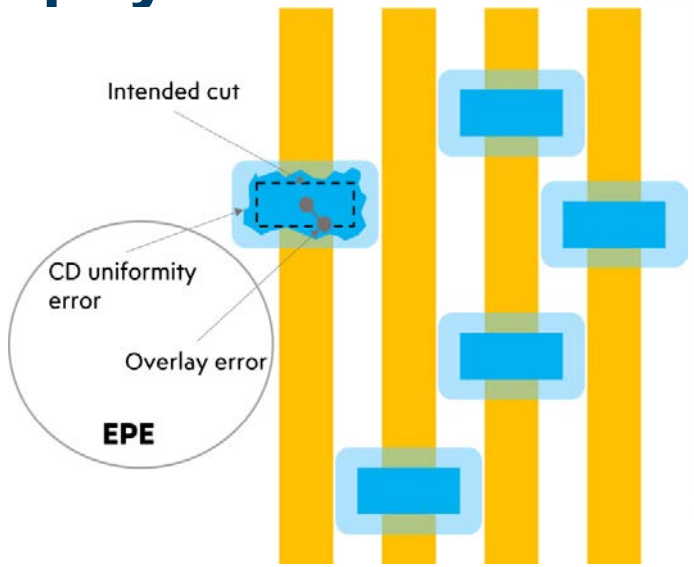
May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

FormFactor™

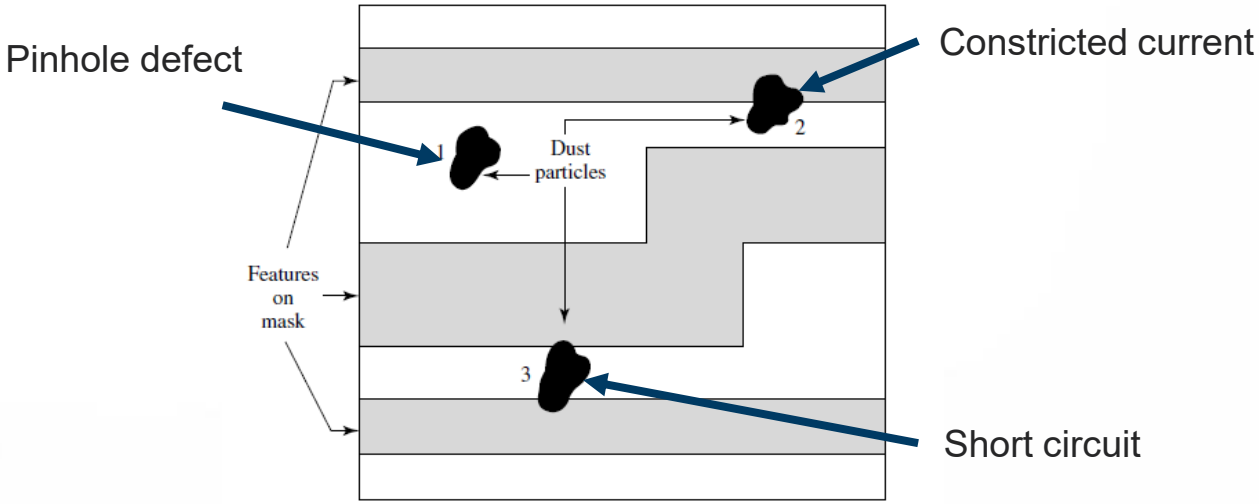
Fab Challenges: Lithography

- Mask defects compound and significantly impact yield
- High resolution means tighter tolerances for registration and uniformity
- Dust can cause a multitude of defects depending on the feature





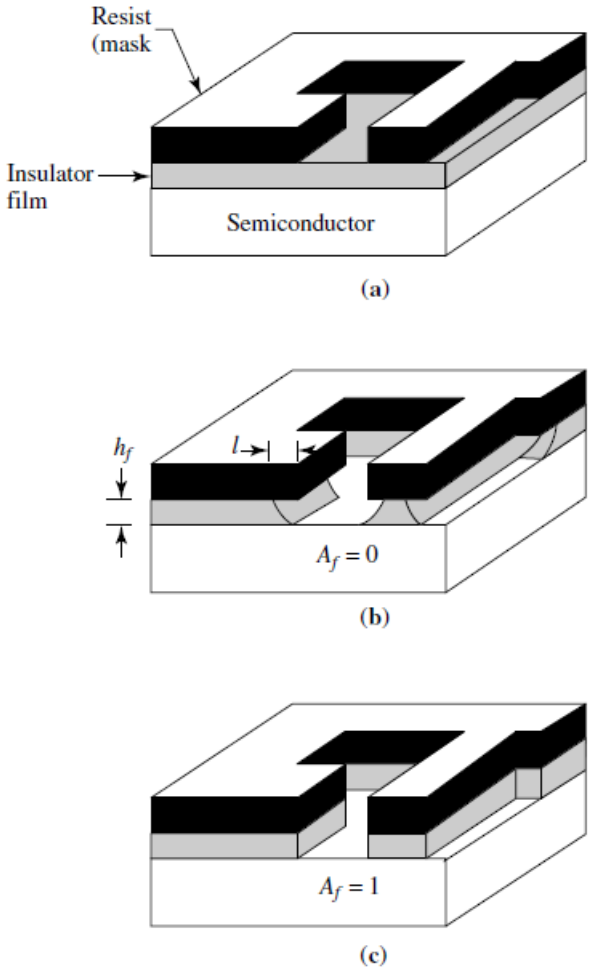
Source: ASML



May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

FormFactor™

Fab Challenges: Etching

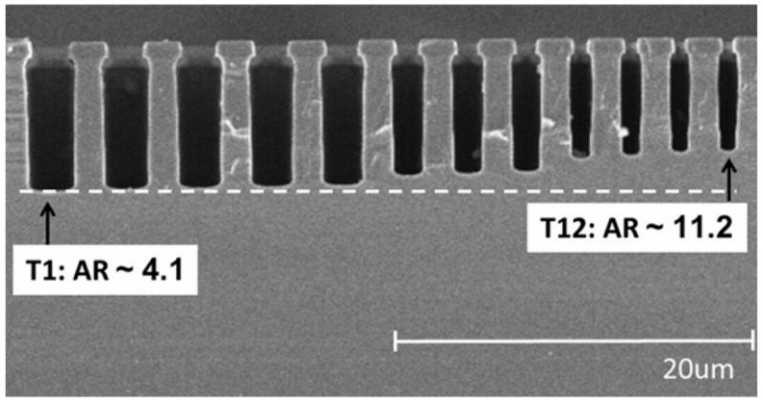


Pattern Transfer

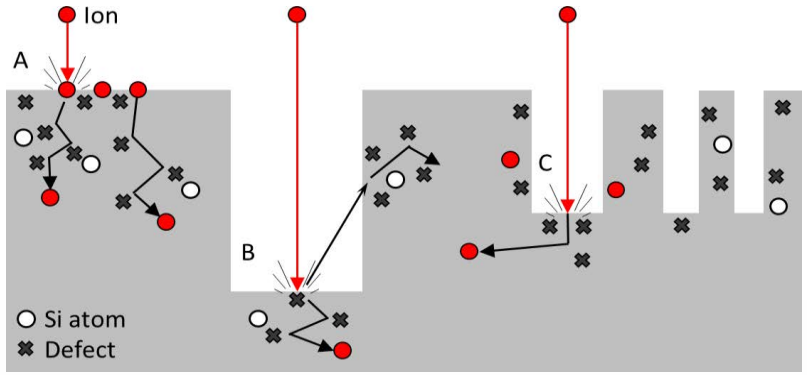
Wet Chemical Etch
Isotropic

Plasma Etch
Anisotropic

- Isotropic etching can lead to undercutting of the photoresist
- Aspect ratio dependent etch rates can lead non-uniform depth
- Plasma induced damage creates defects in subsequent steps



Bates, R. L., Goeckner, M. J., & Overzet, L. J. (2014).



Reiter, T., Klemenschits, X., & Filipovic, L. (2022).

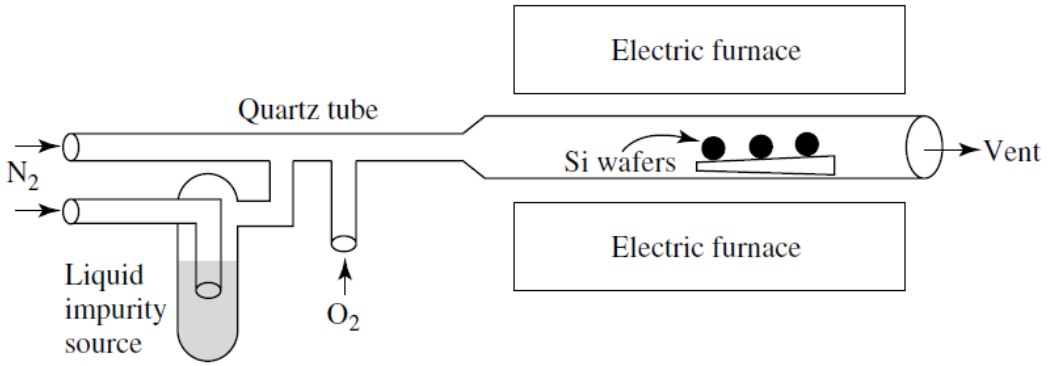
May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

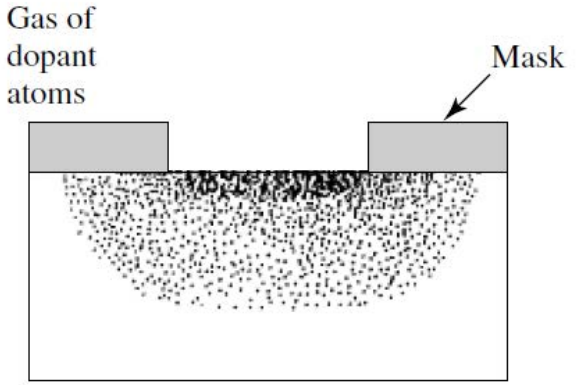
FormFactor™

Fab Challenges: Doping

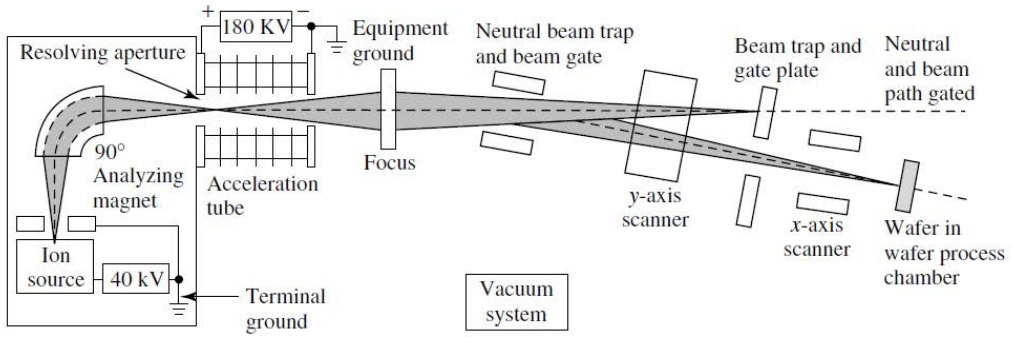
- Doping profile is tightly controlled to limit substrate leakage and parasitic capacitance
- Ion implantation can cause damage to the crystal lattice which requires annealing
- Dopant atoms may settle into interstitial sites rather than displacing the silicon atoms

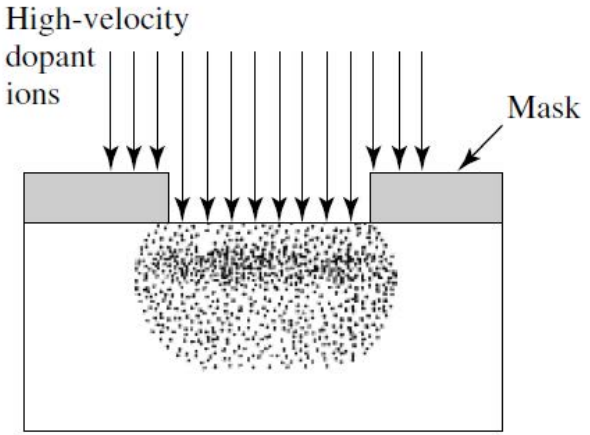
Diffusion





Ion Implantation



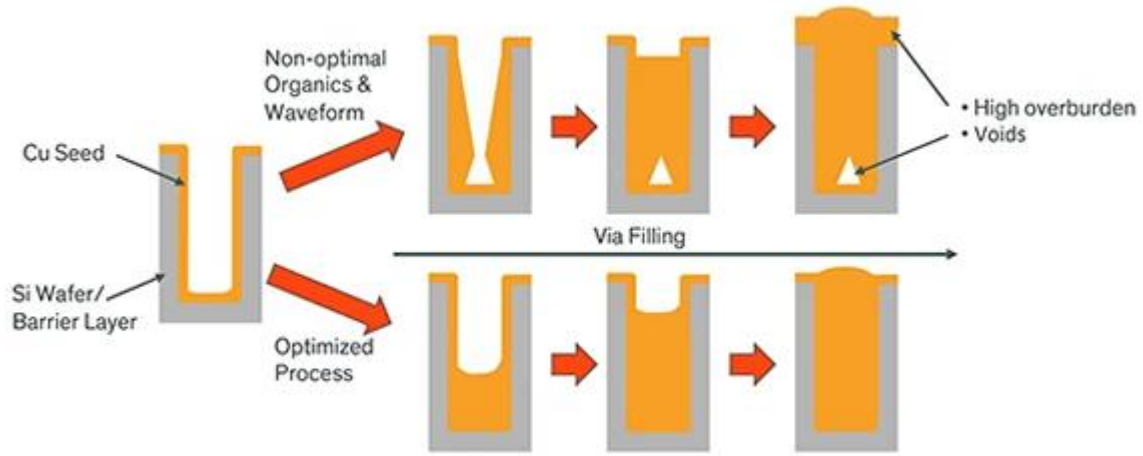


May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

FormFactor™

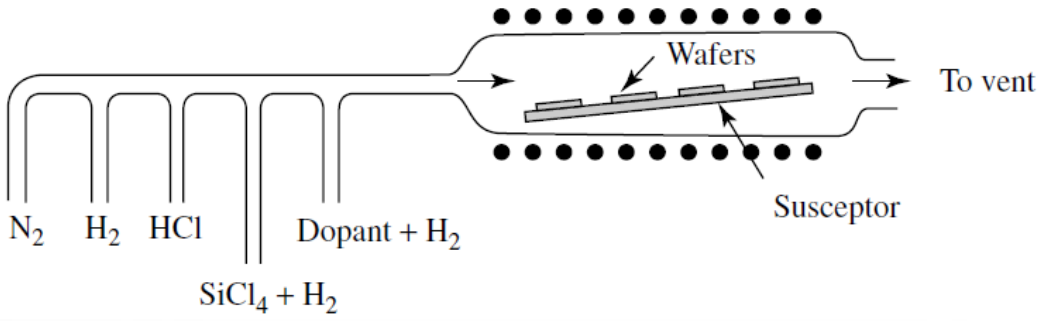
Fab Challenges: Metallization

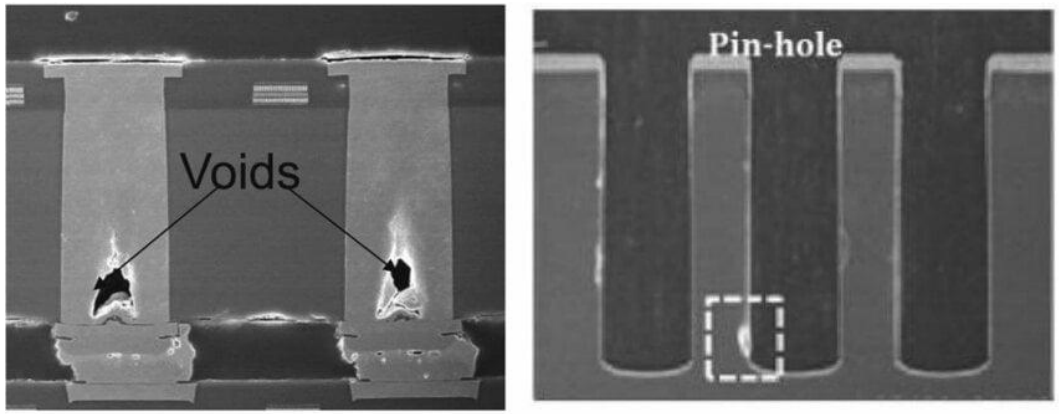
- High aspect ratio features like through silicon vias can have void or pin-hole defects
- Delamination can occur when there is high mechanical stress and low surface adhesion
- Non-conformal film deposition around steps most common in PVD processes



https://www.machining-custom.com/blog/copper-electroplating.html

Chemical Vapor Deposition



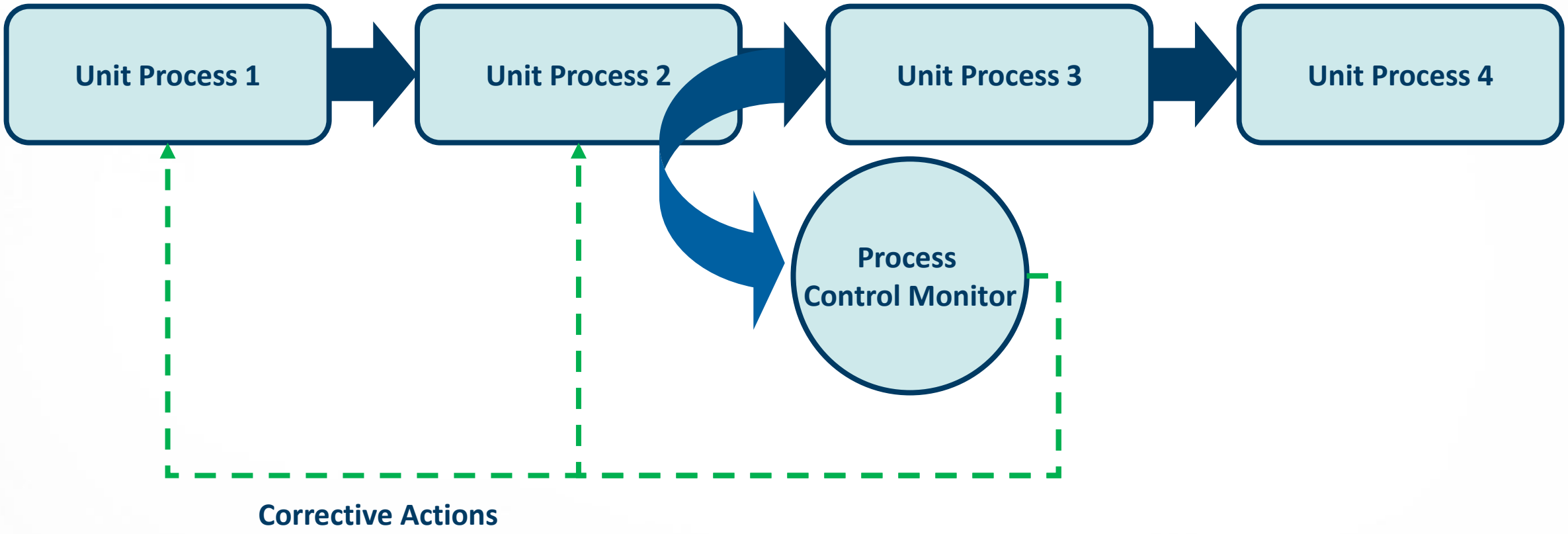


[10] Liu, C., Dong, G., Zhi, C. et al.

May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

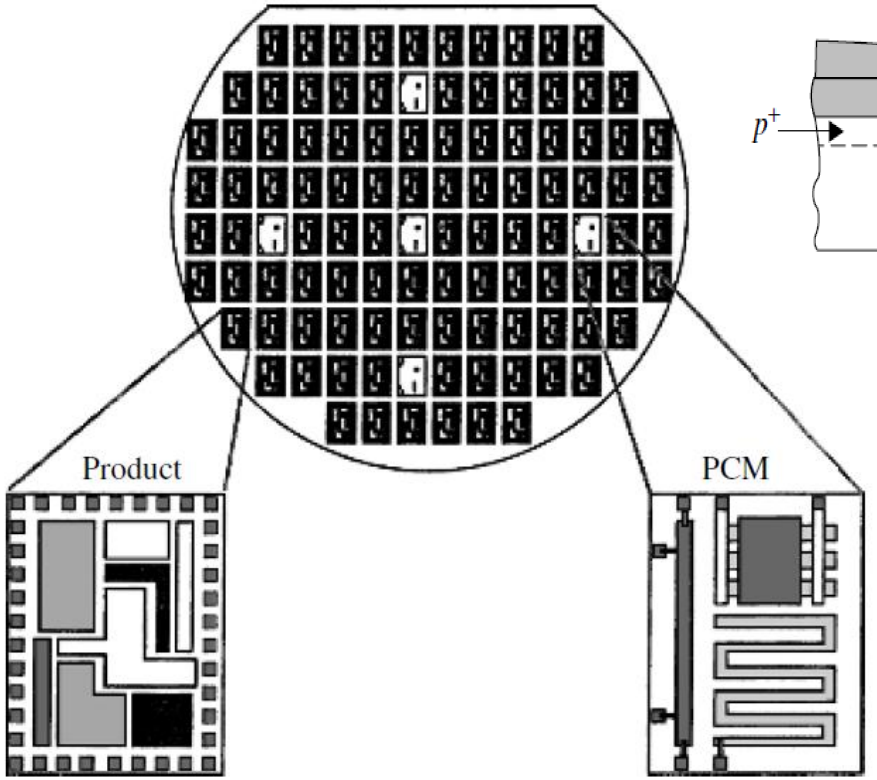
FormFactor™

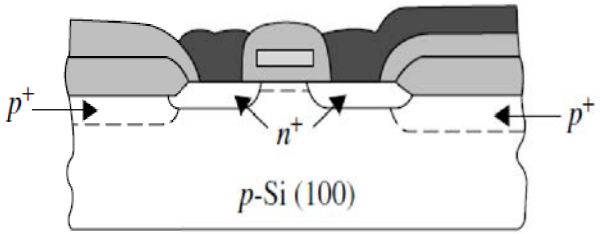
Process Control Monitoring



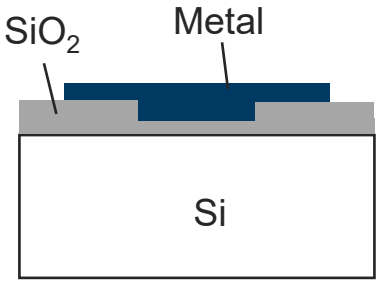
FormFactor™

Process Control Monitoring

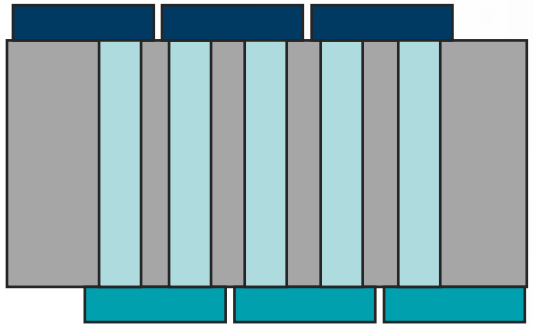




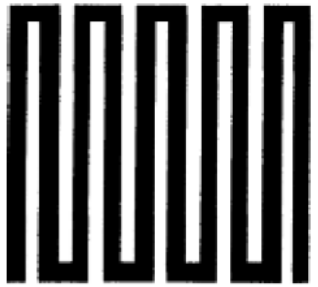
Single Transistor
NMOS/PMOS



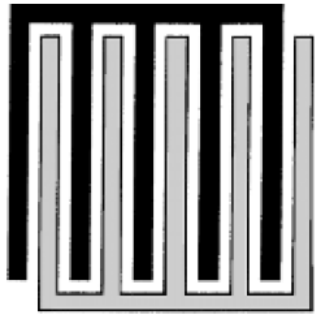
MOS Capacitor
Gate Oxide



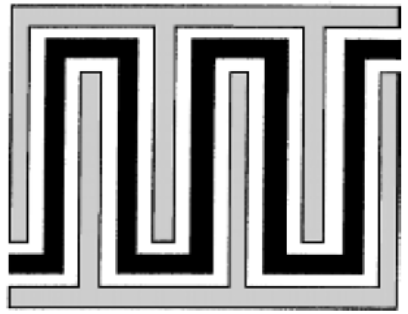
Via Chain
Opens/Shorts



Meander
Opens



Double Comb
Shorts

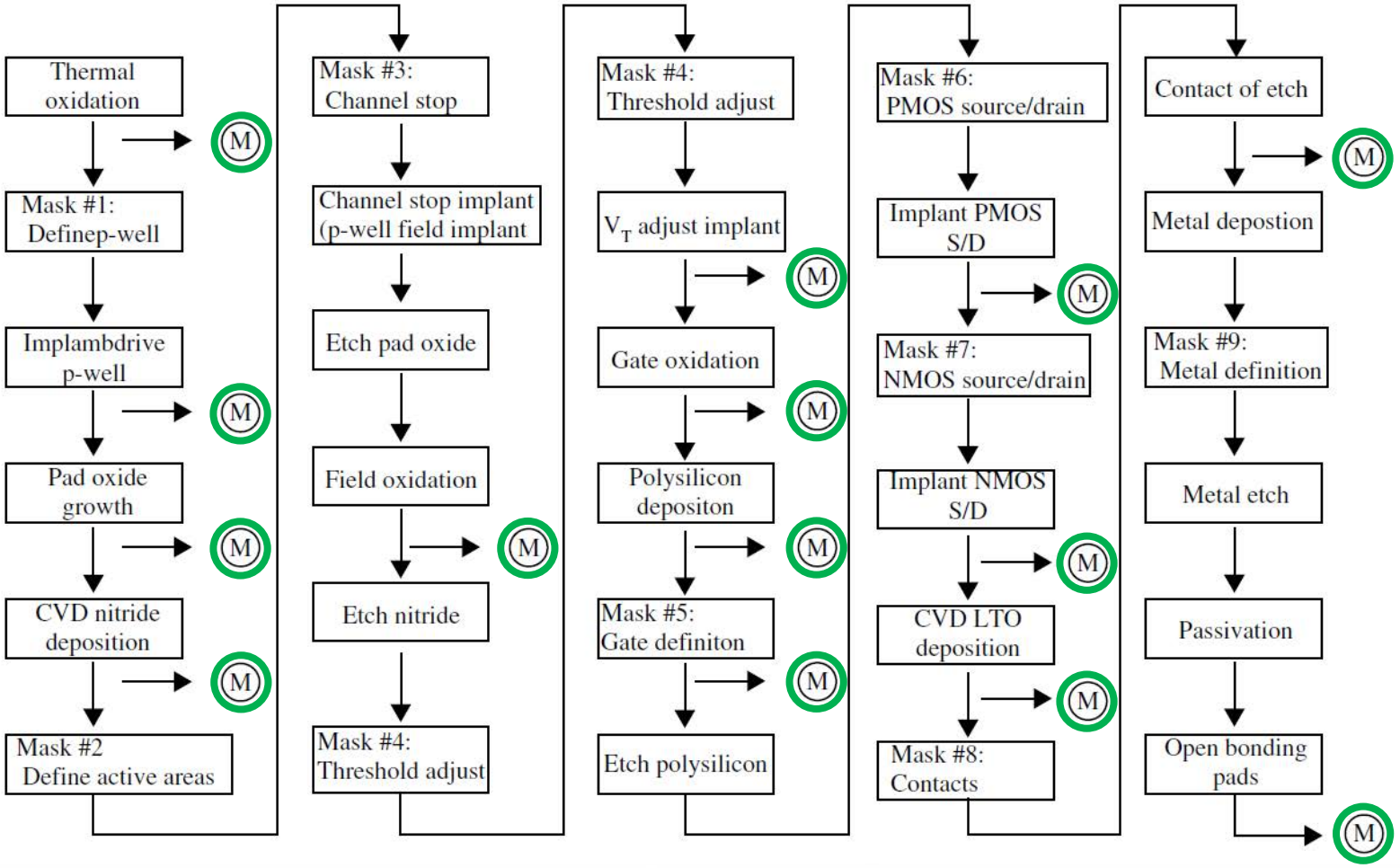


Comb-Meander-Comb
Opens/Shorts

FormFactor™

Process Control Monitoring

Example CMOS Process Flow

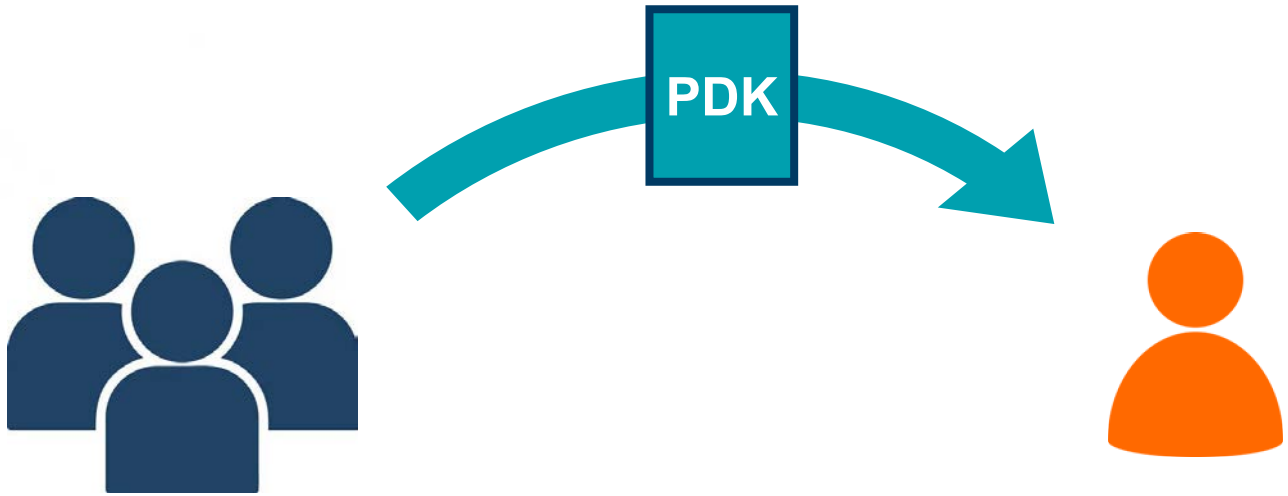


M Process Control Monitors

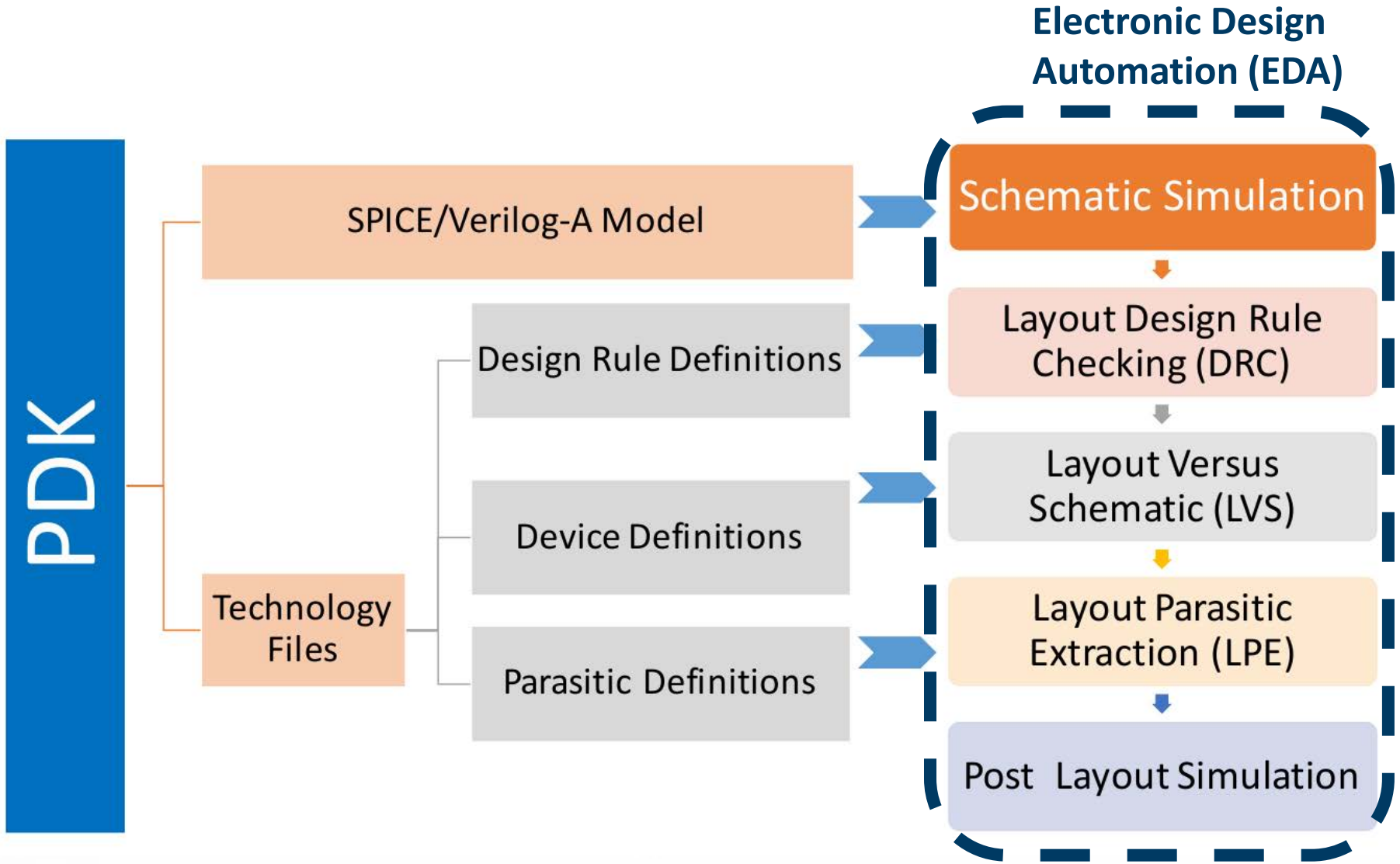
May, G. S., & Spanos, C. J. (2006). *Fundamentals of Semiconductor Manufacturing and Process Control*. Hoboken, NJ: John Wiley & Sons, Inc.

FormFactor™

Process Design Kit



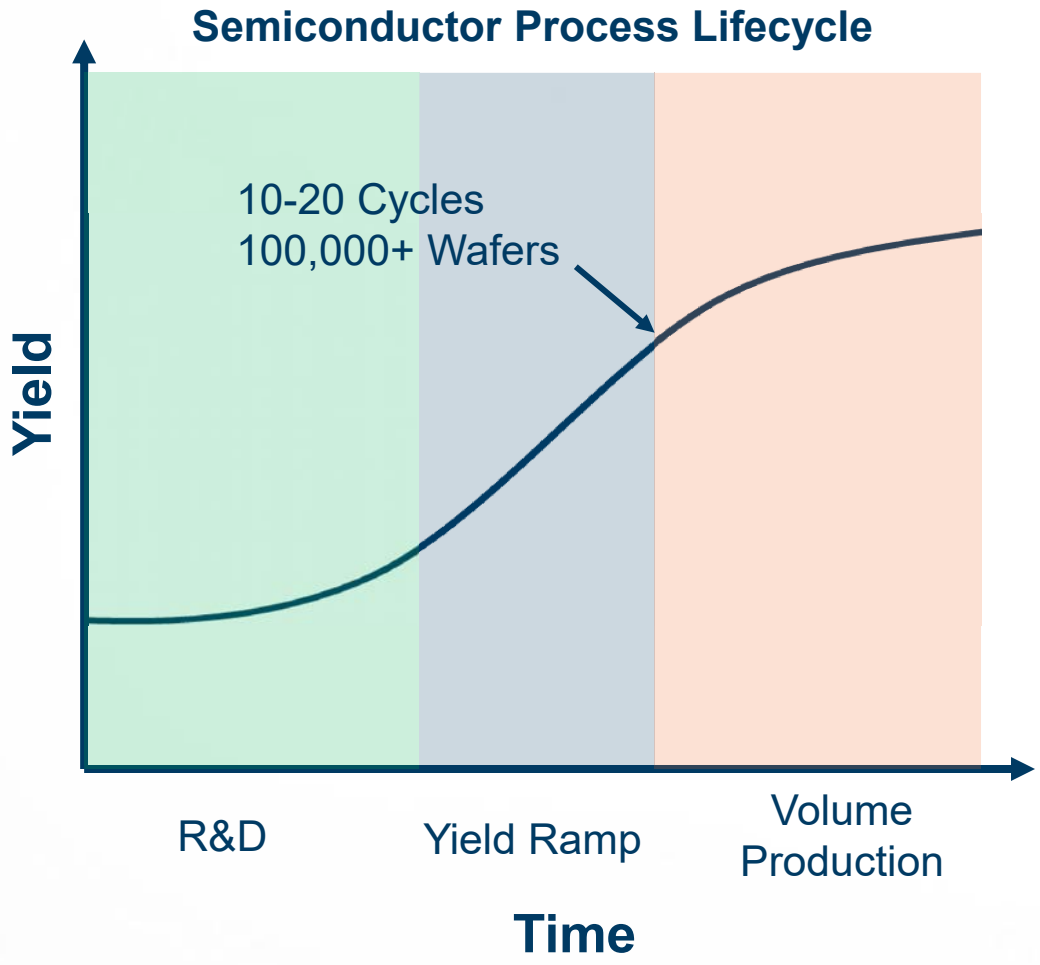
Process Design Kit



[11] Shao, L., Huang, T. C., Lei, T., & Beausoleil, R. G. (2018).

FormFactor™

Process Design Kit

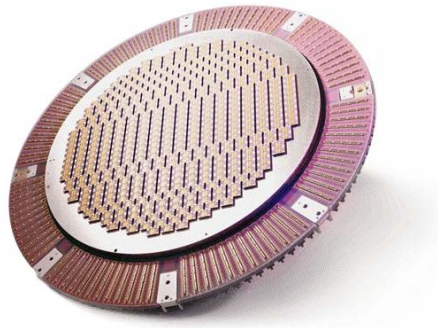




Wafer Probe Station



Automated Test Equipment



Advanced Probe Cards

FormFactor™

Quantum and Cryogenic Technologies

Quantum Computing

Spin Qubits

Trapped Ions

Superconducting Qubits

Photonic Qubits

Neutral Atoms

Quantum Sensing

TES

SQUID

SNSPD

MKID

Readout and Control Electronics

TWPA

JPA

HEMT

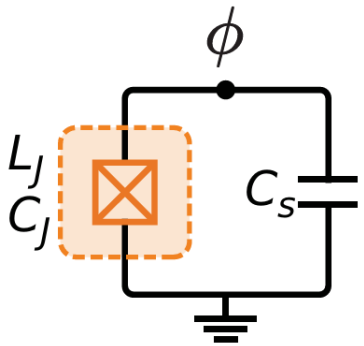
Cryogenic CMOS

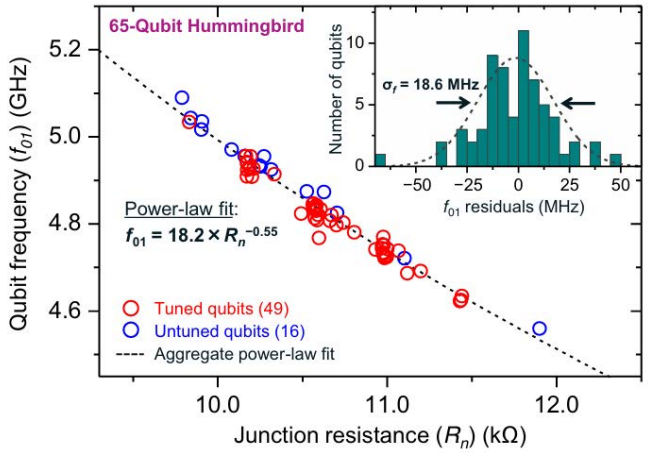
RSFQ Logic

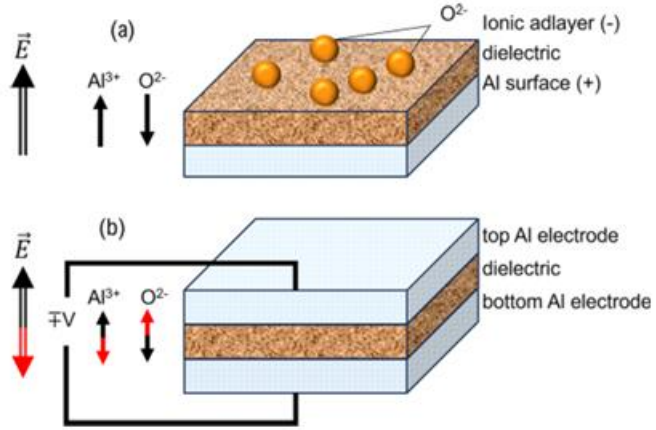
FormFactor™

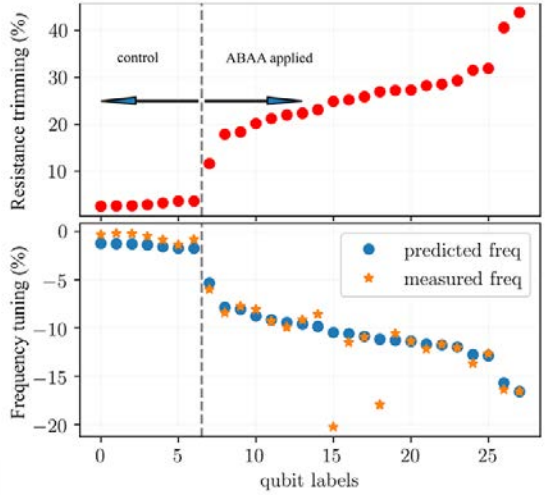
Wafer Testing for Quantum Technology

- Qubit frequency is well correlated to room temperature junction resistance
- Tuning can be performed in-line with fabrication for fixed frequency transmons

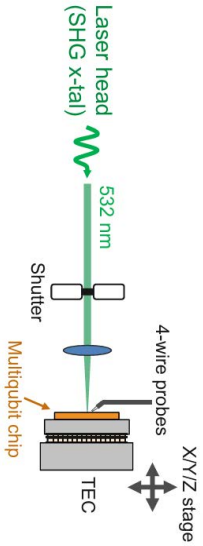


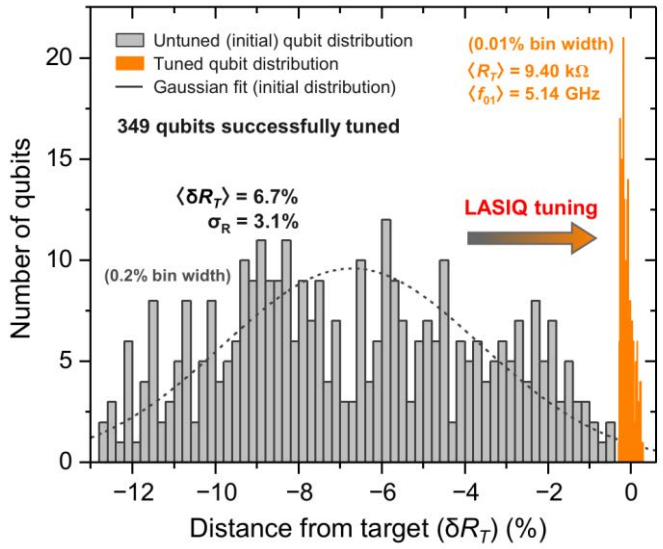






[12] Pappas, D. P. et. al. (2024).



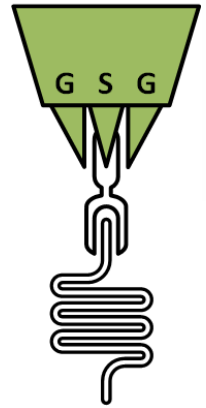


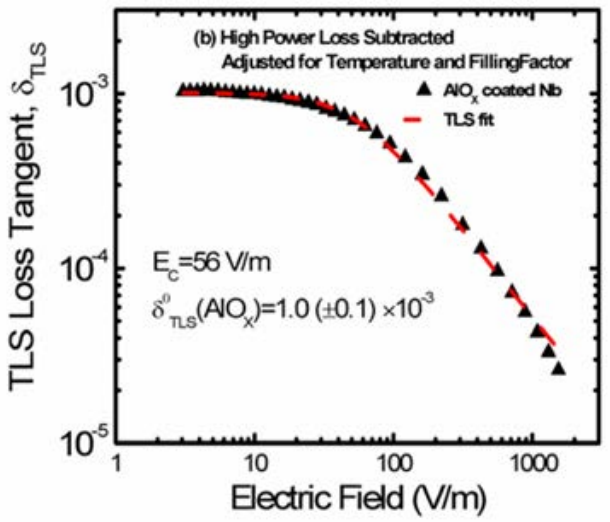
[13] Zhang, E. J. et. al. (2022).

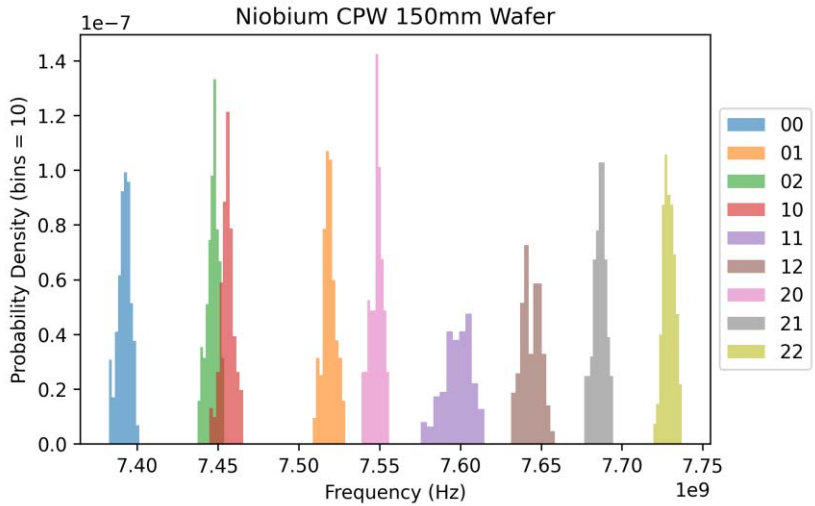
FormFactor™

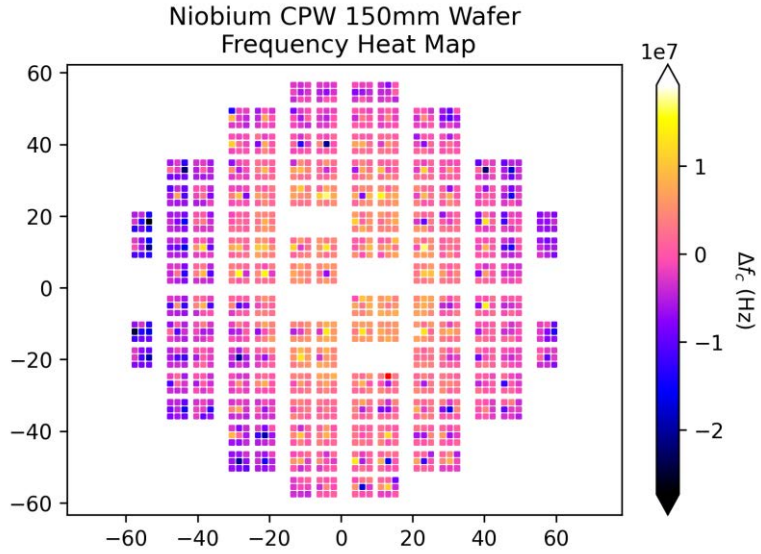
Emergent Cryogenic Properties and Defects

- Properties like superconductivity only emerge at cryogenic temperatures
- Two level systems appear at lower temperatures increasing loss
- Fabrication error and variability translate to readout resonator frequencies
- Statistical analysis on cryogenic data reveals corrective actions





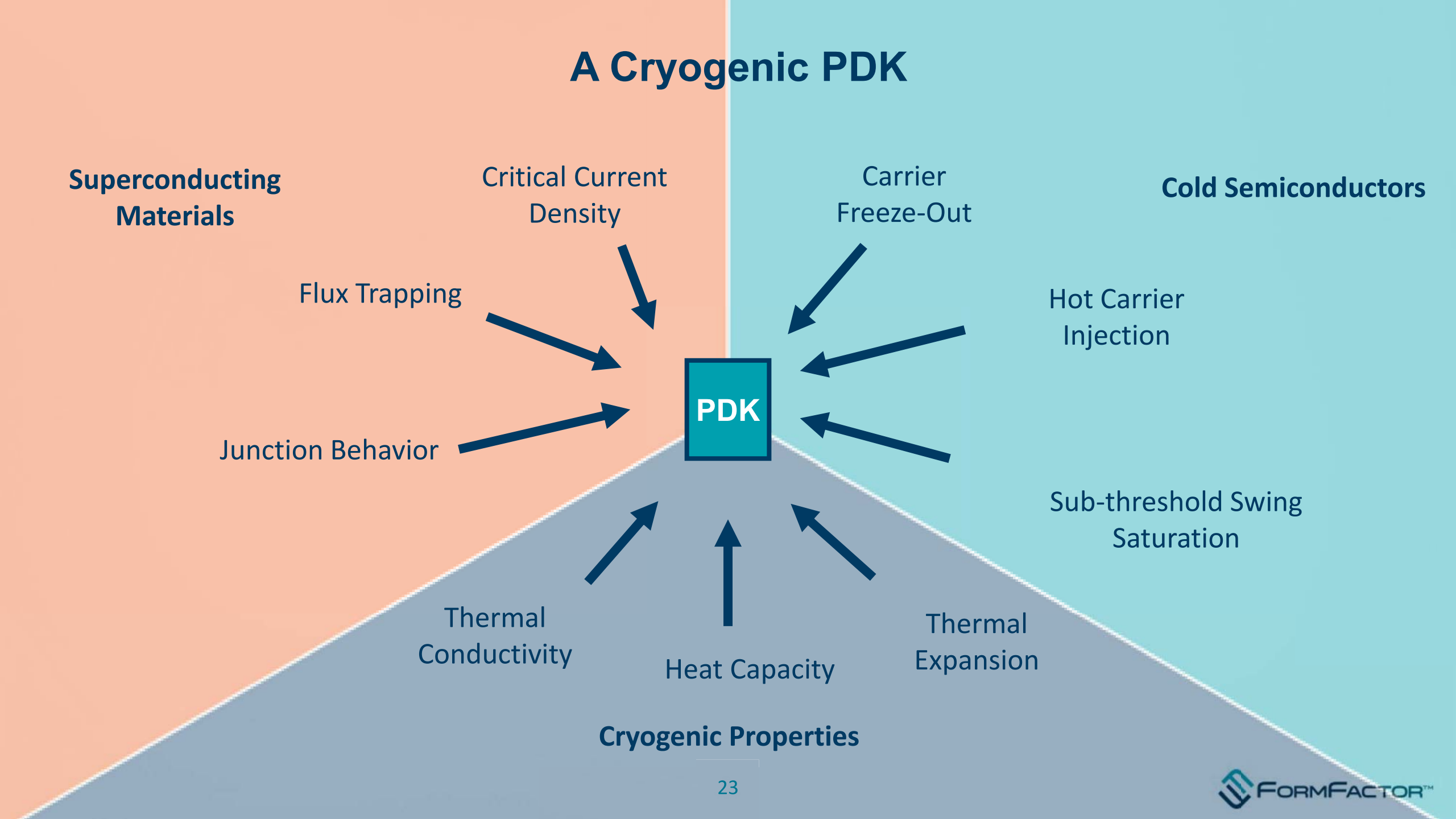




[14] Pappas, D. P., Vissers, M. R., Wisbey, D. S., Kline, J. S., & Gao, J. (2011).

FormFactor™

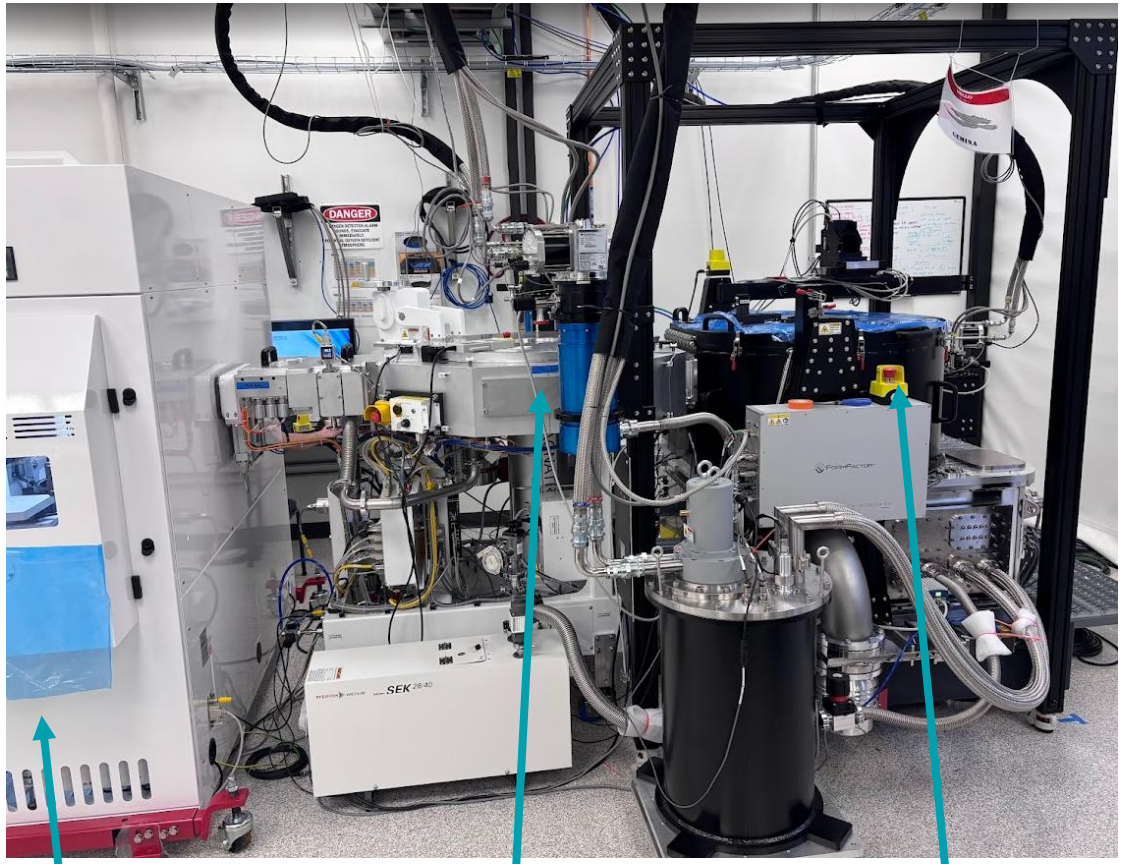
A Cryogenic PDK



FormFactor™

Cryogenic Wafer Scale Probing

HPD IQ3000 4K Cryogenic Wafer Prober

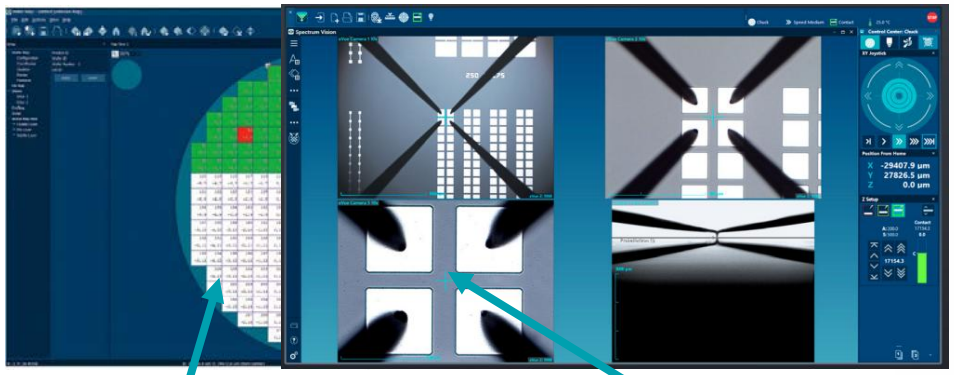


300 mm FOUP Loader

Vacuum Robot and Transfer Chamber

Cryogenic Probe Chamber

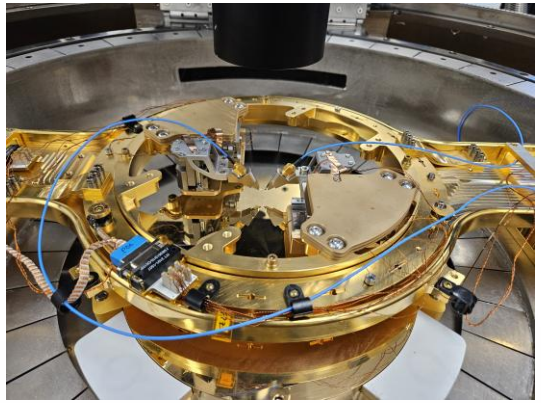
Velox Automated Wafer Probing Software



Automated Wafer Mapping

Auto Re-align and Image Analysis

Cryogenic Quadrant Probe Card



Cryogenic Vertical MEMS Probe Card



FormFactor™

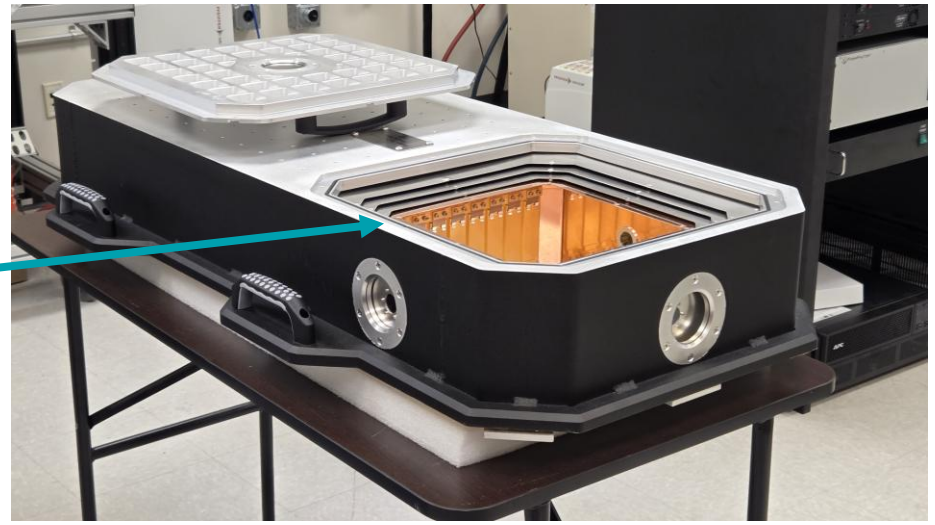
Millikelvin Test and Measurement

HPD Flatiron Tabletop Dilution Refrigerator



Modular Wiring Blades

Gas Handling System



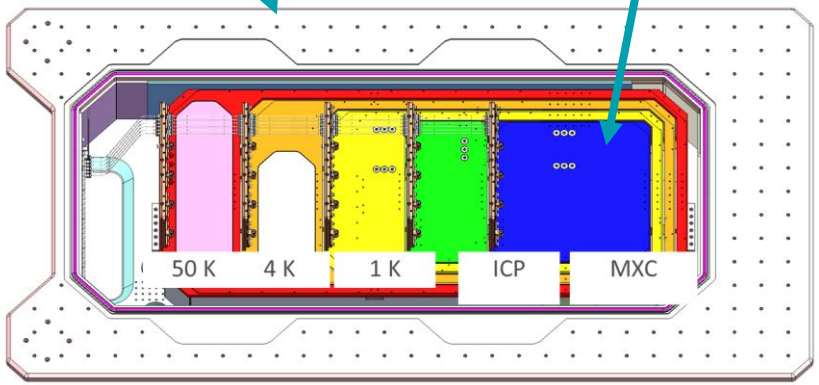
Sample Access Port

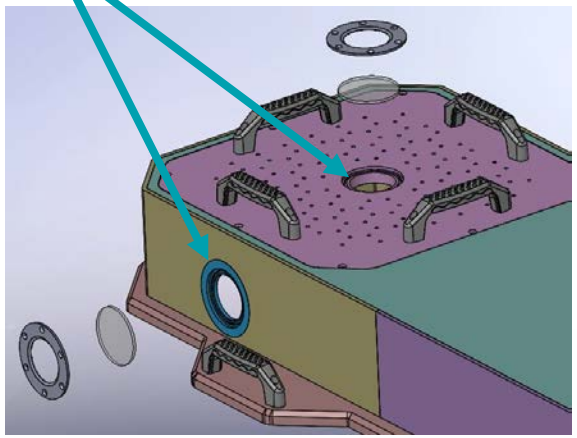
Optical View Ports

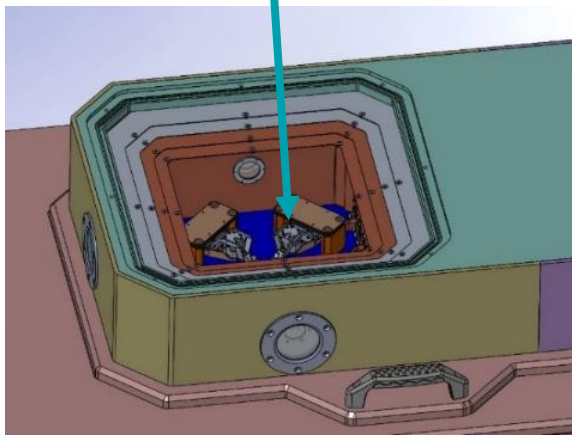
Probing with Nanopositioners

Optics Table

Cold Space
300 mm x 300 mm x 125 mm

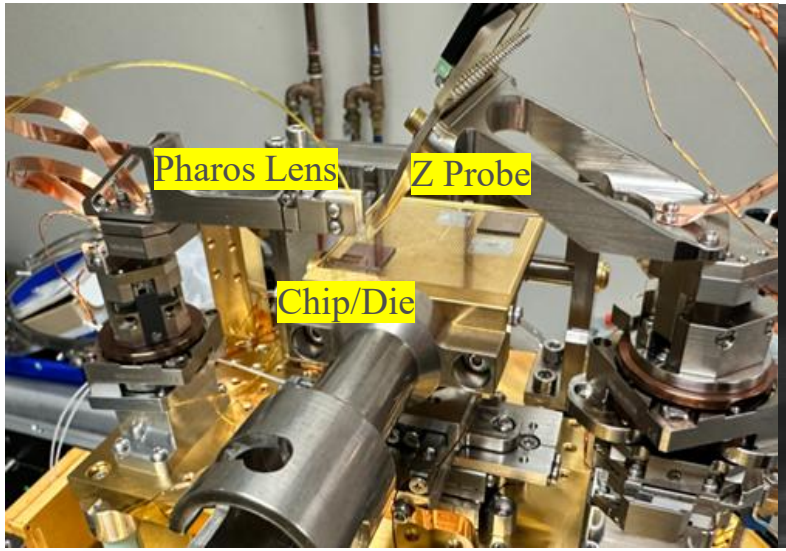


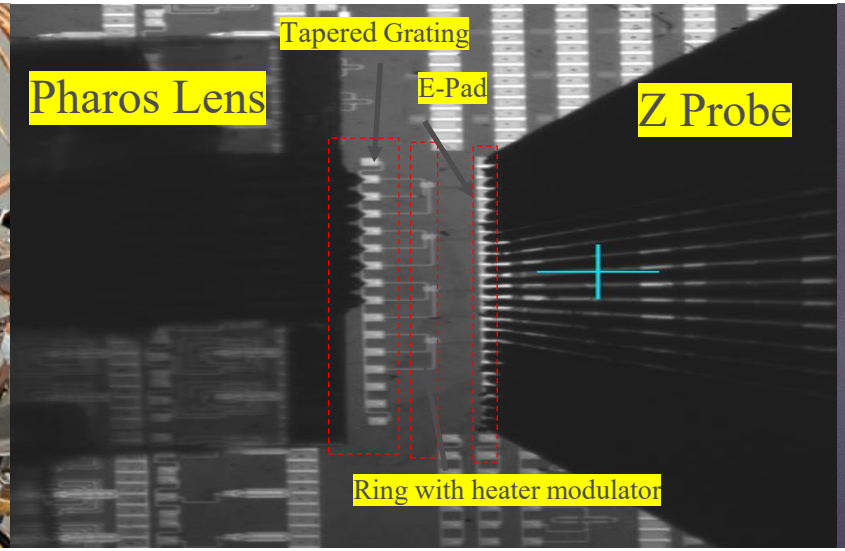




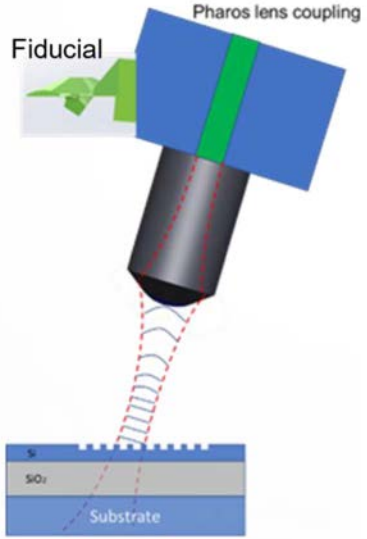
FormFactor™

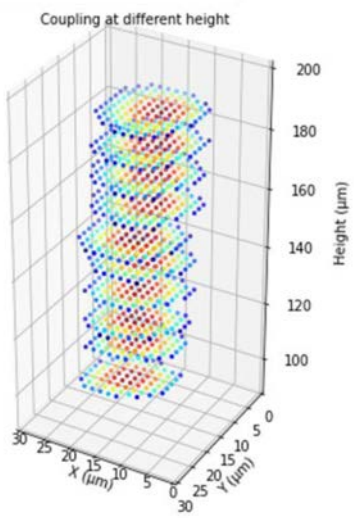
Cryogenic Photonic Probing

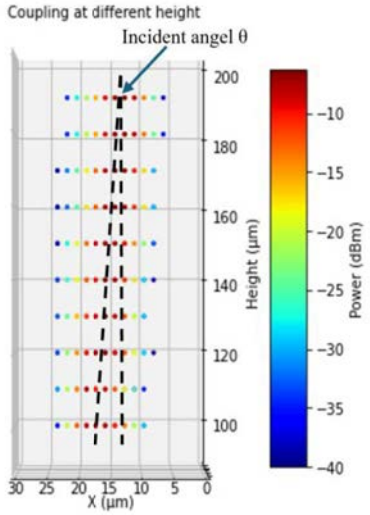


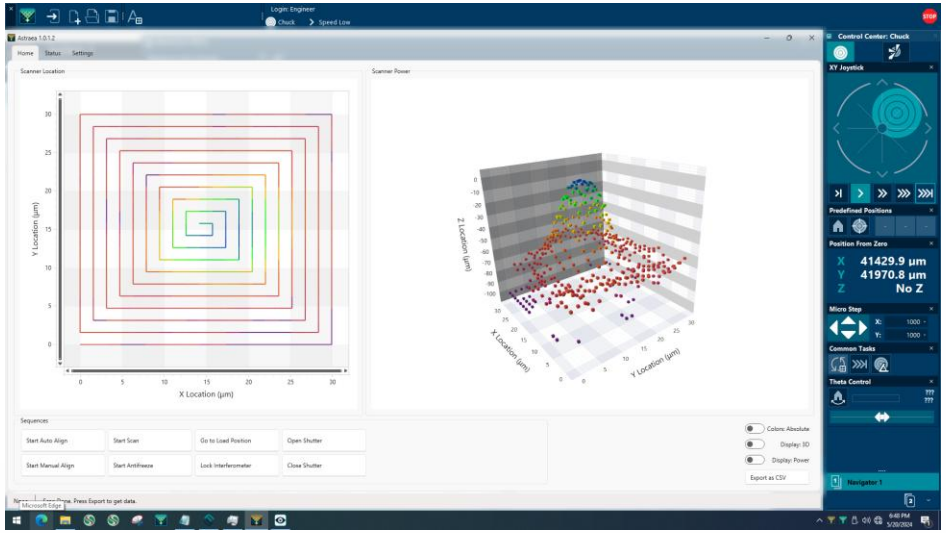












FormFactor™

Summary

- Brief history of semiconductor fabrication and provided an overview of the manufacturing processes
- Discussed the goals of a semiconductor process and established a concept of process control monitoring
- Explained what Process Design Kits (PDKs) are and the tools needed to create them.
- Reviewed quantum and cryogenic technologies and explored some common defects
- Introduced the concept of a cryogenic PDK encompassing superconducting materials and cryogenic semiconductors
- Presented technology developments in cryogenic test and measurement

FormFactor™

References

[1] Roser, M., & Ritchie, H. (2020). Transistor count over time [Graph]. Our World in Data. https://ourworldindata.org/uploads/2020/11/Transistor-Count-over-time.png

[2] Jurvetson, S. (2024, December 3). The Moore's Law update — for 128 years. Steve Jurvetson. https://steve.blog/2024/12/03/the-moores-law-update-for-128-years/

[3] Semiconductor manufacturing flow steps: Layer-build loop. (n.d.). SemiconductorX. Retrieved June 8, 2026, from https://semiconductorx.com/semiconductor-manufacturing-steps.php

[4] May, G. S., & Spanos, C. J. (2006). Fundamentals of Semiconductor Manufacturing and Process Control. Hoboken, NJ: John Wiley & Sons, Inc.

[5] Weber, C. (2004). Yield learning and the sources of profitability in semiconductor manufacturing and process development. IEEE Transactions on Semiconductor Manufacturing, 17(4), 590–596.

[6] LaPedus, M. (2017, March 20). Patterning problems pile up. Semiconductor Engineering. https://semiengineering.com/patterning-problems-pile-up/ [1]

[7] Bates, R. L., Goeckner, M. J., & Overzet, L. J. (2014). Correction of aspect ratio dependent etch disparities. Journal of Vacuum Science & Technology A, 32(5), Article 051302. doi.org

[8] Reiter, T., Klemenschits, X., & Filipovic, L. (2022). Impact of plasma induced damage on the fabrication of 3D NAND flash memory. Solid-State Electronics, 192, Article 108261. doi.org

[9] Machining-Custom. (2025, January 6). Copper electroplating: Working principle, advantages, and common applications. https://www.machining-custom.com/blog/copper-electroplating.html

[10] Liu, C., Dong, G., Zhi, C. et al. Modelling and simulation of TSV considering void and leakage defects. J Comput Electron 24, 61 (2025). https://doi.org/10.1007/s10825-025-02300-x

[11] Shao, L., Huang, T. C., Lei, T., & Beausoleil, R. G. (2018). Process design kit for flexible hybrid electronics. Proceedings of the 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), 651–657. doi.org

[12] Pappas, D. P., Field, M., Kopas, C. J., Howard, J. A., Wang, X., Lachman, E., Zhou, L., Oh, J., Yadavalli, K., Sete, E. A., Bestwick, A., Kramer, M. J., & Mutus, J. Y. (2024). Alternating-bias assisted annealing of amorphous oxide tunnel junctions. Communications Materials, 5(1).

[13] Zhang, E. J., Suresh, S., Abdo, B., Córcoles, A. D., Gallagher, M. J., Keefe, G. A., Brink, M., Chow, J. M., & Steffen, M. (2022). High-performance superconducting quantum processors via laser annealing of transmon qubits. Science Advances, 8(19), eabi6690. doi.org

[14] Pappas, D. P., Vissers, M. R., Wisbey, D. S., Kline, J. S., & Gao, J. (2011). Two level system loss in superconducting microwave resonators. IEEE Transactions on Applied Superconductivity, 21(3), 871–874. doi.org