Is Parametric Testing About to enter a Period of Growth and Innovation?

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IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Agenda

- Parametric test
- Trends
- Summary

DC Production Parametric Testing Overview

Upwards of 1000 facilities worldwide do semiconductor wafer processing. Around 2000 parametric testers are used in those sites, 750 of which are obsolete. That is, the system vendor has stated they no longer provide new versions, no longer update software, and will only repair on a best-effort basis.

Reedholm 8/2009

DC Parametric Test

"As the dimensions of modern integrated circuits continue to shrink and the use of innovative material grows, device fabrication and parametric testing have become more challenging in each passing year."

Flavio Riva ST Microelectronics Keithley Parallel Test Technology handbook

As process technologies continually advance, local process variation has greatly increased and gradually become one of the most critical factors for IC manufacturing. To monitor local process variation, a large number of DUTs (devices under- Test) in close proximity must be measured.

(A novel array-based test methodology for local process variation monitoring ITC 2009 Tseng-Chin Luo etal)

New Directions In Parametric and Defect Structure Testing

Variability Challenges at 22 nm and Beyond

- Spreads in basic parameters (like V_t) are becoming worse. Larger statistics are required.
- Test time for process monitoring can't grow.
- The manufacturing process must be economically viable.
- Need to improve test efficiency *(what is tested; how we test) :*

IBM 300 mm Manufacturing Facility, East Fishkill N.Y.

2010 SWTW R. Robertazzi (IBM Research)

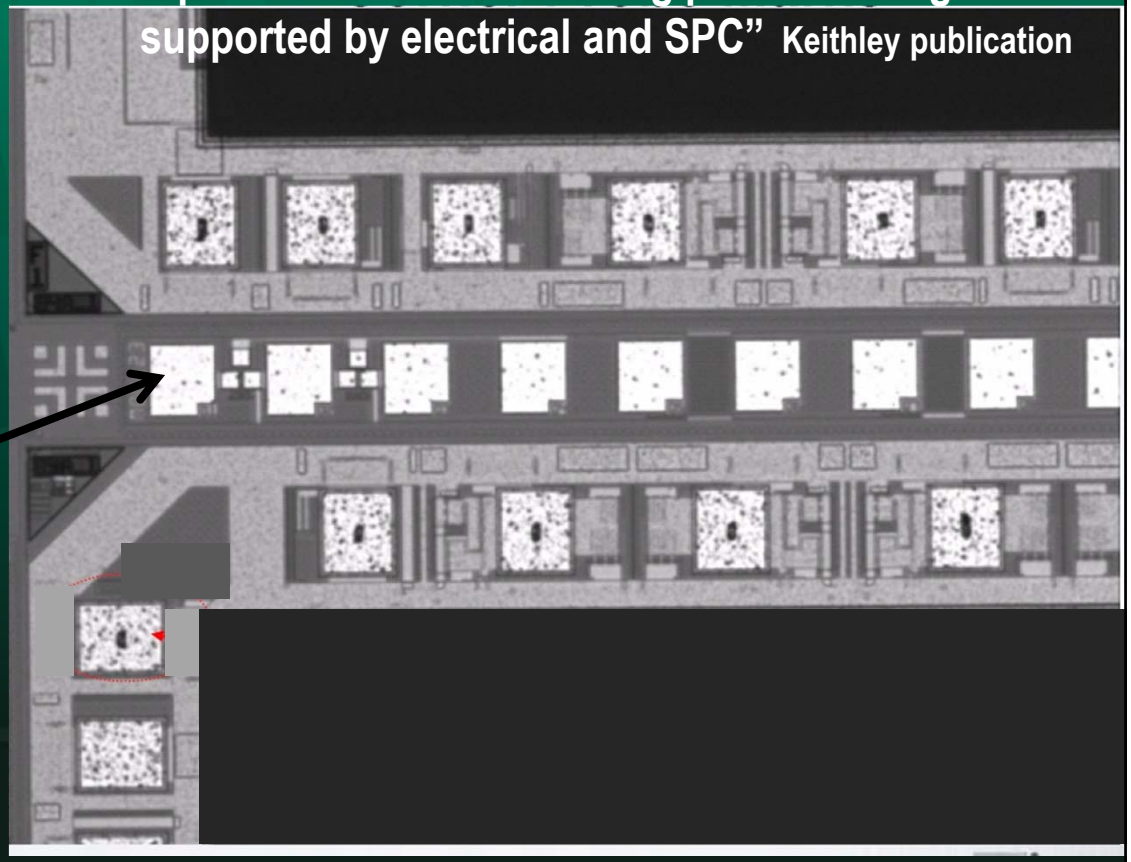
DC Parametric Test

- **For simplicity we can split DC parametric test into three categories**
  - In Line
    - While wafer probing has been used for in-line e-test for more than a decade, its effectiveness in high-volume manufacturing environments has been severely limited by the probe card generating contamination and or particles
  - End of Line
  - Quality and reliability (WAT)

Parametric Pads

"Typical scribe line test structures are components and grouping of components that represent the manufacturing process being supported by electrical and SPC" Keithley publication

Test pads/structures (PCM's) in the kerf between dies
Pads are usually arranged in one direction only for reuse of probe cards



DC Parametric Testers

No new testers introduced for many years

Agilent

Reedholm

Keithley

S600 series no longer supported starting this year

Some parametric testers have been in continual use for over 20 years- Reedholm

DC Parametric Testing Trends

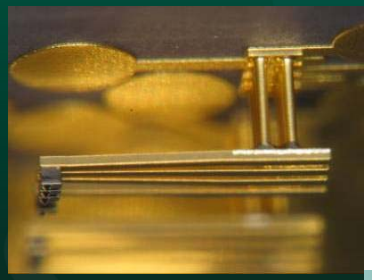
Typical DC parametric tests are not changing

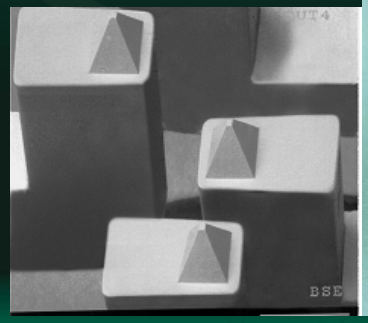
- **JFET Gate Current Measurements**
- **High Resistivity (>5MΩ) Measurements**
- **Breakdown Voltage Tests Including Bipolar Transistors**
- **BVceo Breakdown Measurements**
- **Measuring RDSon and VCEsat in Biased Chuck Systems**

- **Typical DC probe card requirements have been fairly constant**
  - Low leakage
    - Typically 1pA/ 10V @ 1 sec or 250 fA @ 10 sec
  - Repeatability and stability of the measurement
    - Low CRES
  - Low particle generation
  - Small scrub mark becoming more critical as pad sizes shrink

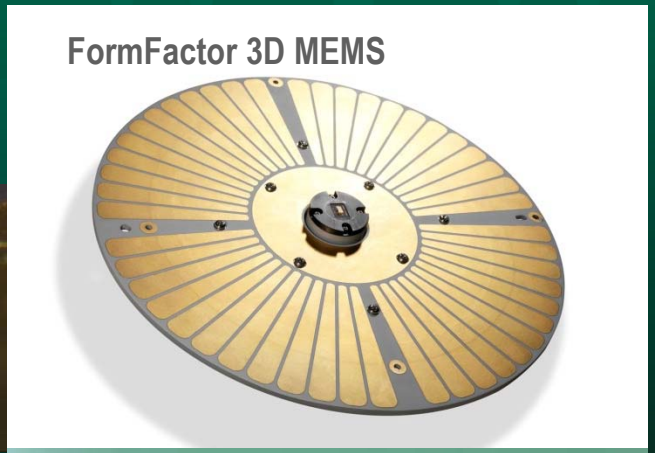
DC Parametric Probe Cards

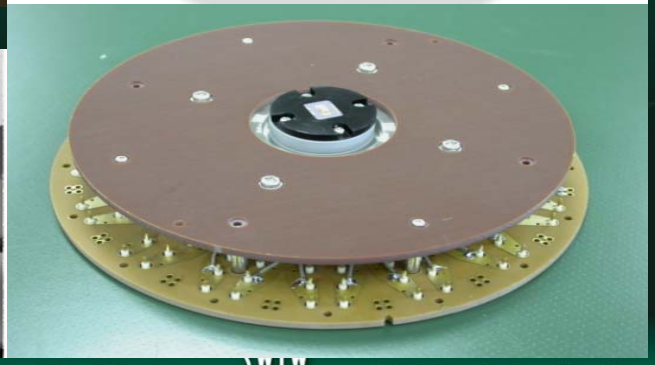
Many choices
- Traditional needle cards
- Membrane cards
- 3D MEMS cards



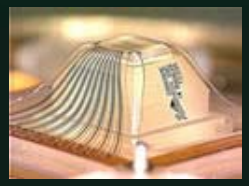


FormFactor 3D MEMS



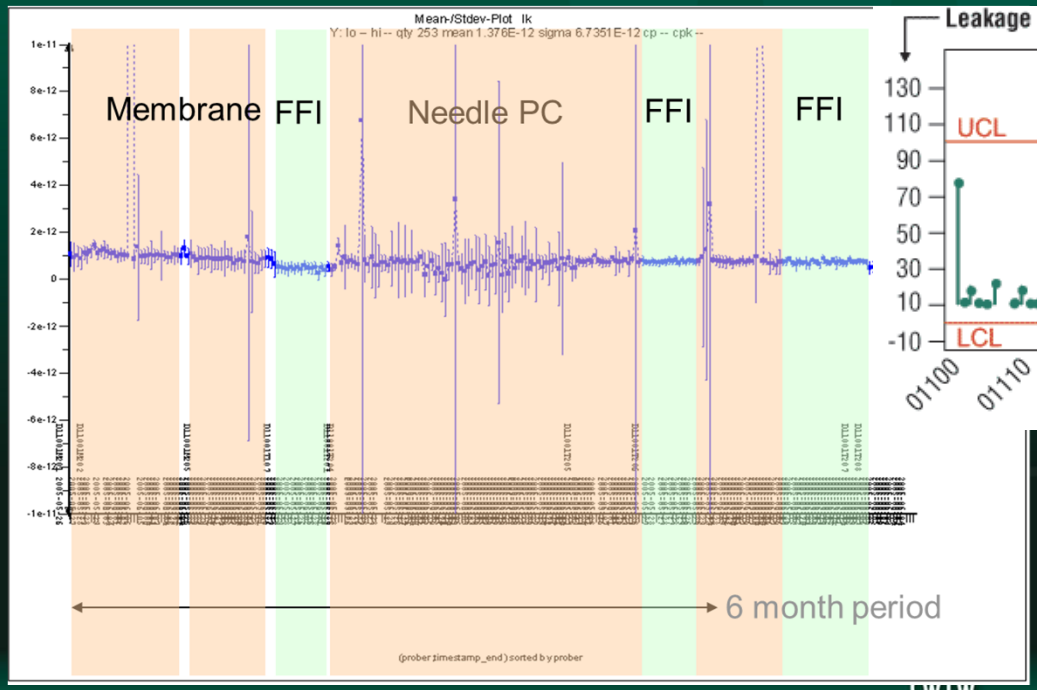


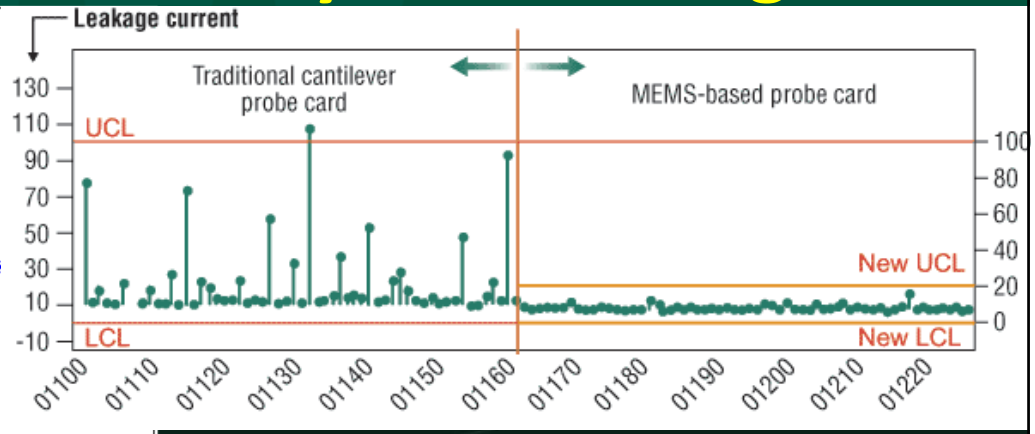
Membrane by Cascade Microtech



DC Parametric Low Leakage

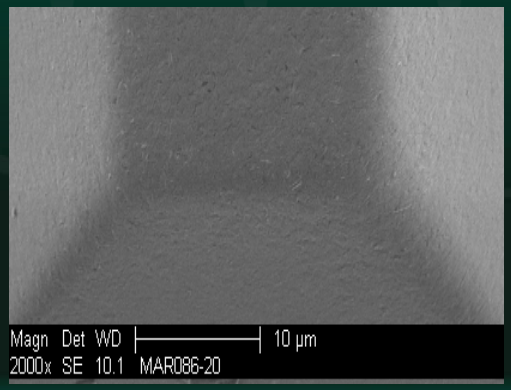
- Most probe card solutions can meet the low leakage requirements
- Stability and accuracy of the measurements enable feedback and faster yield learning





Contamination and Particles

- The probing process generates particles
- Rather than do inline tests many companies resort to using visual methods to find defects
  - Can this continue as geometries shrink?
- There are technologies that can reduce particles



Customers reported 3x less particles using MEMS springs versus needles

DC Parametric Test Trends

Trends
Pad size
Pad Pitch
Number of Pads
Test time
Voltage
Temperature
Amount of data collected

DC Parametric Pad Size and Pitch Trend

- **Over the years pad sizes and pitch have been trending smaller**
- **Currently we have seen pad sizes anywhere between 70um Sq to 25um octagonal**
- **Pad pitch has been getting smaller too (100um-→70um)**
  - In some cases probe card capability is limiting the move to smaller pads

DC Parametric Pad Size and Pitch Trend

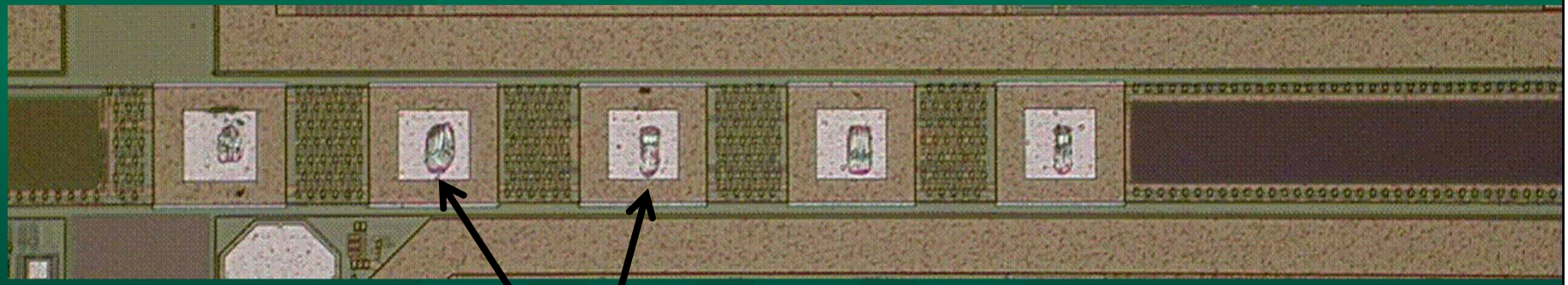
Probes sliding off the pad can lead to "False Fails"

Requiring retest

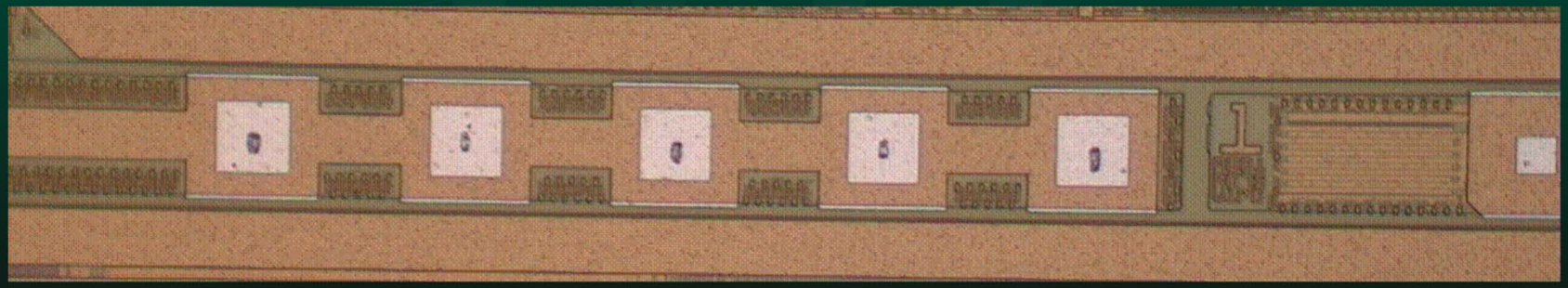
Probes sliding off the pads can damage die if there is no protective oxide

Relative size and impact of a MEMS contactor on a test pad (scrub marks on upper left, upper right, and center right) compared to a cantilever needle (scrub mark at center). Multiple touchdowns with the MEMS contactor are achieved on the same pad with no interlayer dielectric damage

DC Parametric Pad Size and Pitch Trend



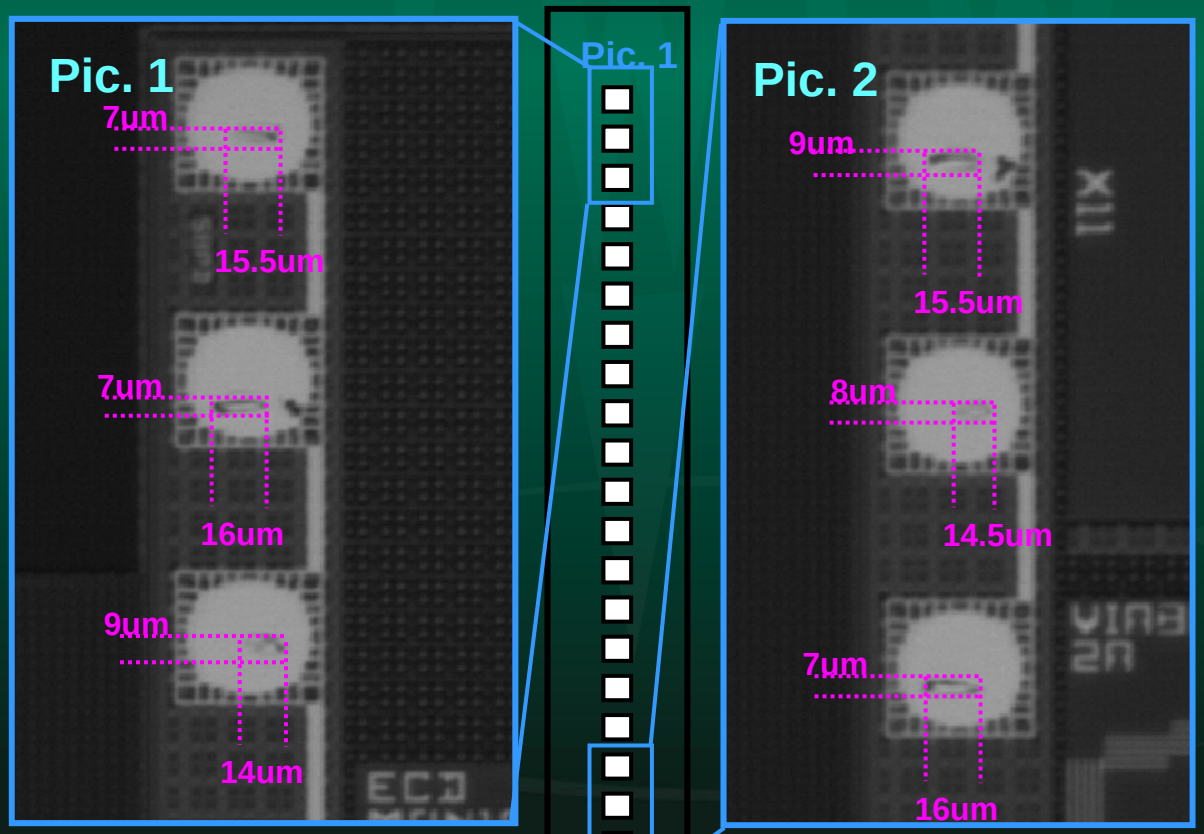
Probe marks at or near the edge of on 40um pad

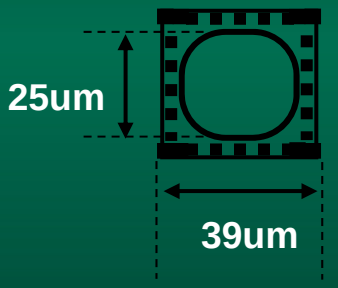


Good probe marks on 50um pads

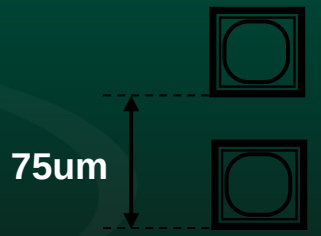
DC Parametric Pad Size and Pitch Trend

Smallest Pad Size Known to be in Production





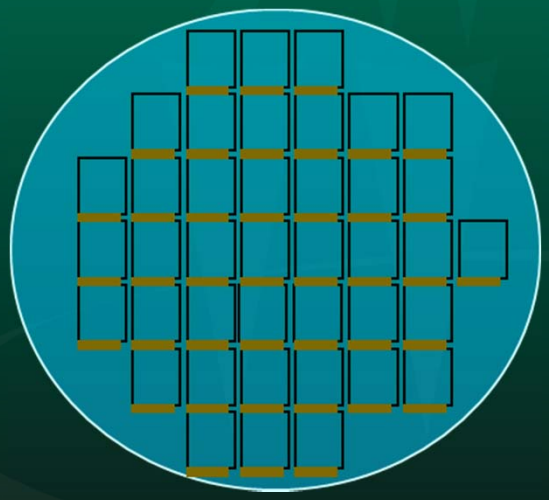
Pad Pitch size



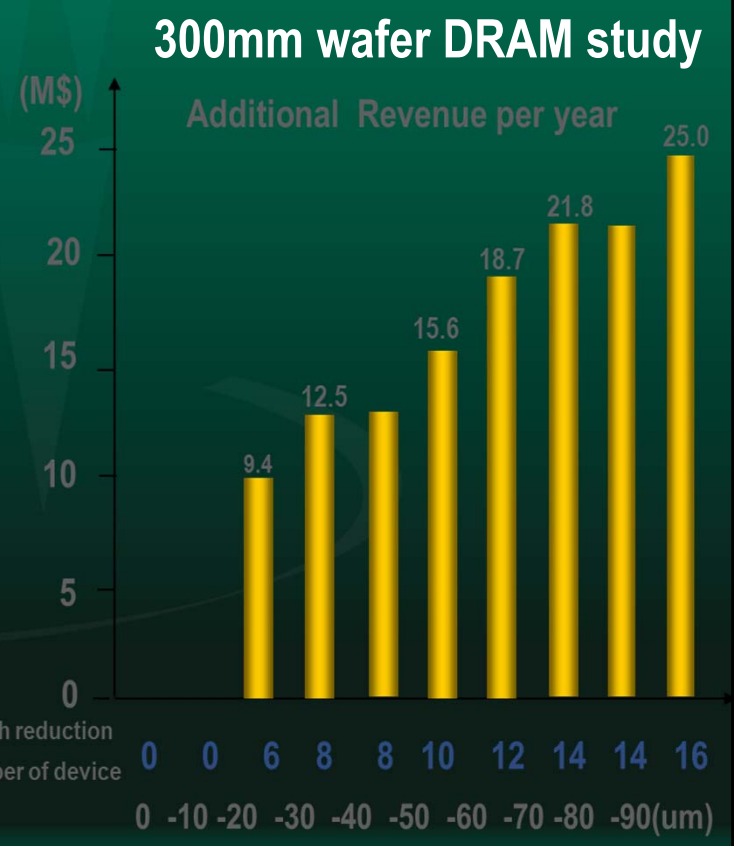
Two companies currently requesting 20um pad capability

DC Parametric Pad Size Trend

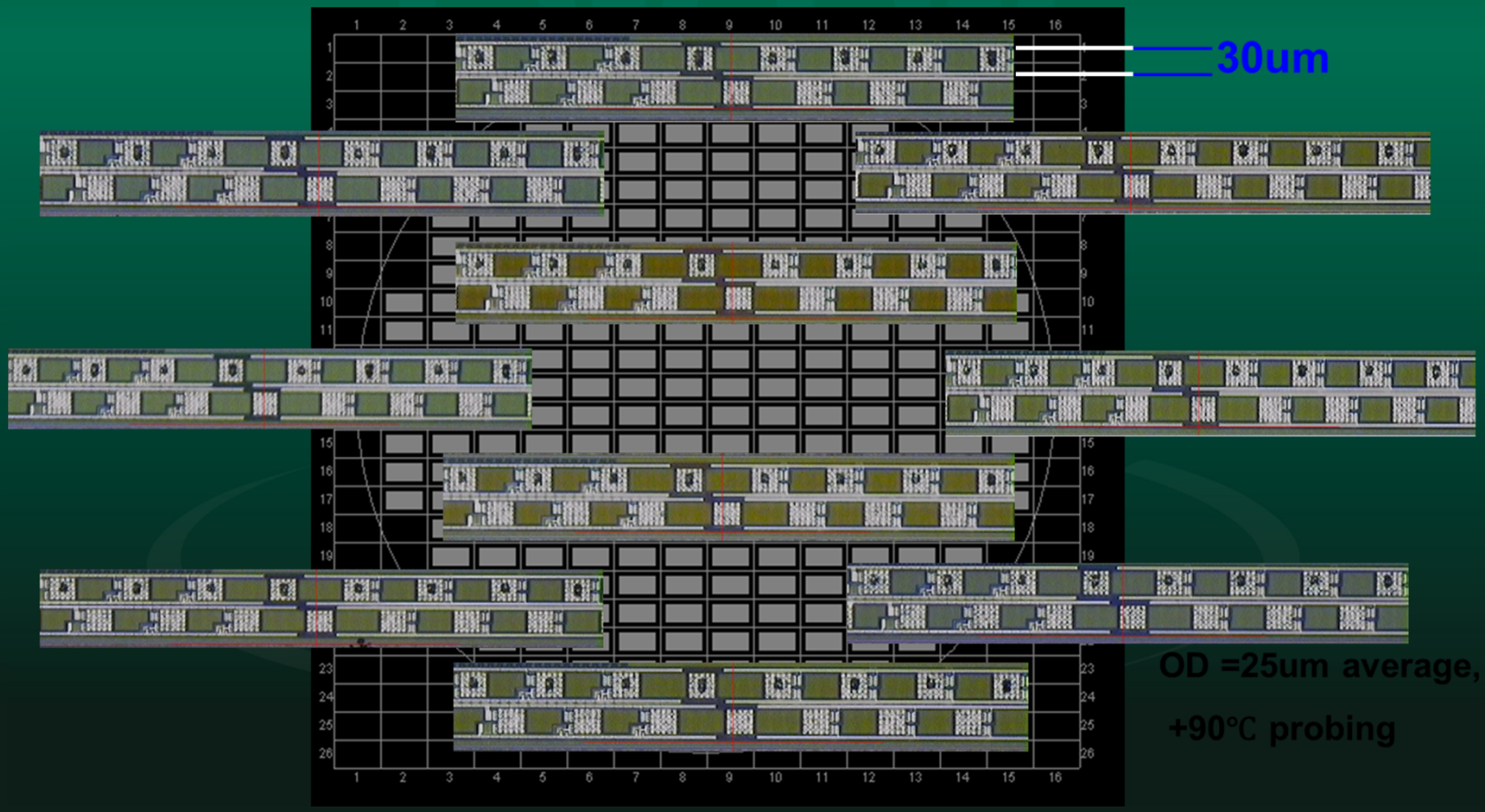
- **Why the trend to smaller pads?**
  - More die per wafer



  - Room for more pads in the scribe line



300mm 30um Pad Parametric Test



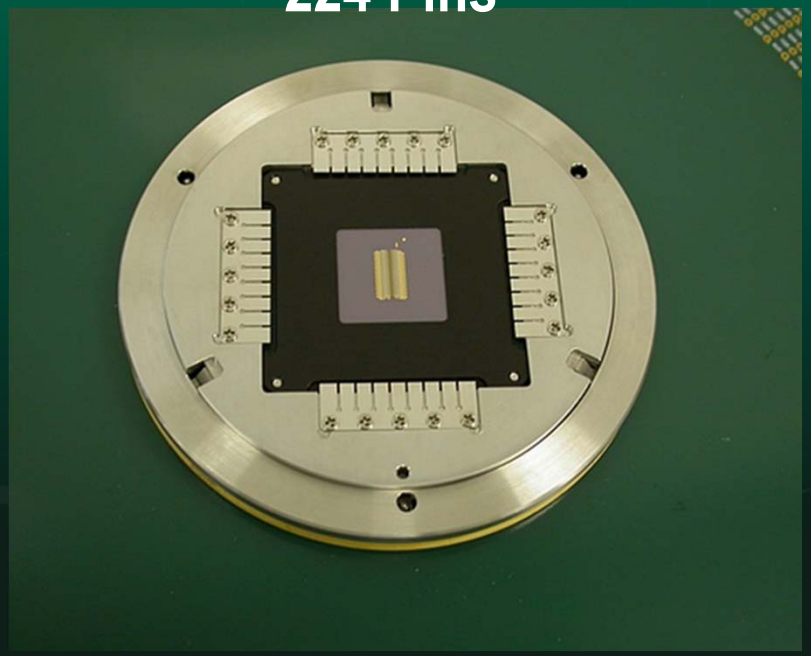
Trend of the Number of DC Parametric Pads Used

- **Most commonly used testers have up to 48 channels**
- **Many are not fully loaded**
- **Average is ~ 22 pads in the scribe line**
  - Drop in structures can be used as well
- **No detectable trend to increase the number of pads being used**

DC Parametric Pad Size and Pitch Trend

- **Non-traditional yield management parametric testing can use much larger pin counts**

224 Pins



DC Parametric Test Time Trend

- **Test times are closely guarded**
- **Some companies simply scrap wafers if parametric test fails**
  - Most do a more rigorous and time consuming retest
- **It appears that test times have remained stable**
  - Reducing retest and other methods (parallel test) have allowed more test data to be collected in the same amount of time

DC Parametric Test Votage and Temperature Trend

- **Increasing Voltage and Temperature are used to further stress the structures**
  - We have experienced 200C requirements for reliability testing
    - Future requirements at 300C???
  - We have seen requests up to 1500V for standard production

Trend of Amount of DC Parametric Data Collected

- **There seems to be a given amount of time for parametric test today**
  - If more data is required the tests needs to be faster or multi sites tested at one time
    - 3D MEMS probe cards have been shown to reduce test times by 21% due to reduced cleaning
    - 3D MEMS cards have been shown to reduce resort re-test rates by 5% to 14%

DC Parametric Test Trends

	Trend
Pad size	Shrinking
Number of Pads	Stable
Pad Pitch	Shrinking
Test time	Stable?
Voltage	Higher
Temperature	Higher
Amount of data collected	Increasing

DC parametric test appears to be slowly changing

As the feature size of devices scales down, the device variability imposed by each process step does not scale accordingly. As a result, the process variation of advanced process technology nodes has greatly increased and has become a critical factor in both IC design and manufacturing (A novel array-based test methodology for local process variation monitoring ITC 2009 Tseng-Chin Luo etal)

DC Parametric Test Trends

- **What about 450mm wafers?**
  - More data will need to be taken due to larger area
  - Local variations will need to be monitored
  - Test times will not be allowed to increase dramatically

Summary

- **DC parametric testing is slowly changing**
  - Temperature and Voltage are leading indicators
  - Seeing some hints of change such as pad size and pitch
- **3D MEMS probe cards can help**
  - 3 D MEMS probe cards can reduce test times versus needle cards by producing stable results
  - 3 D MEMS probe cards can enable smaller pads/pitches enabling more pads to be placed in the same area
  - 3 D MEMS cards can generate less particles
- **New testers will need to be developed**
  - Test faster
  - Test more pads