IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

INNOVATION PUT TO THE TEST

FORMFACTOR

Advanced Wafer Probe Solutions

"Pay it Forward", is it worth it?

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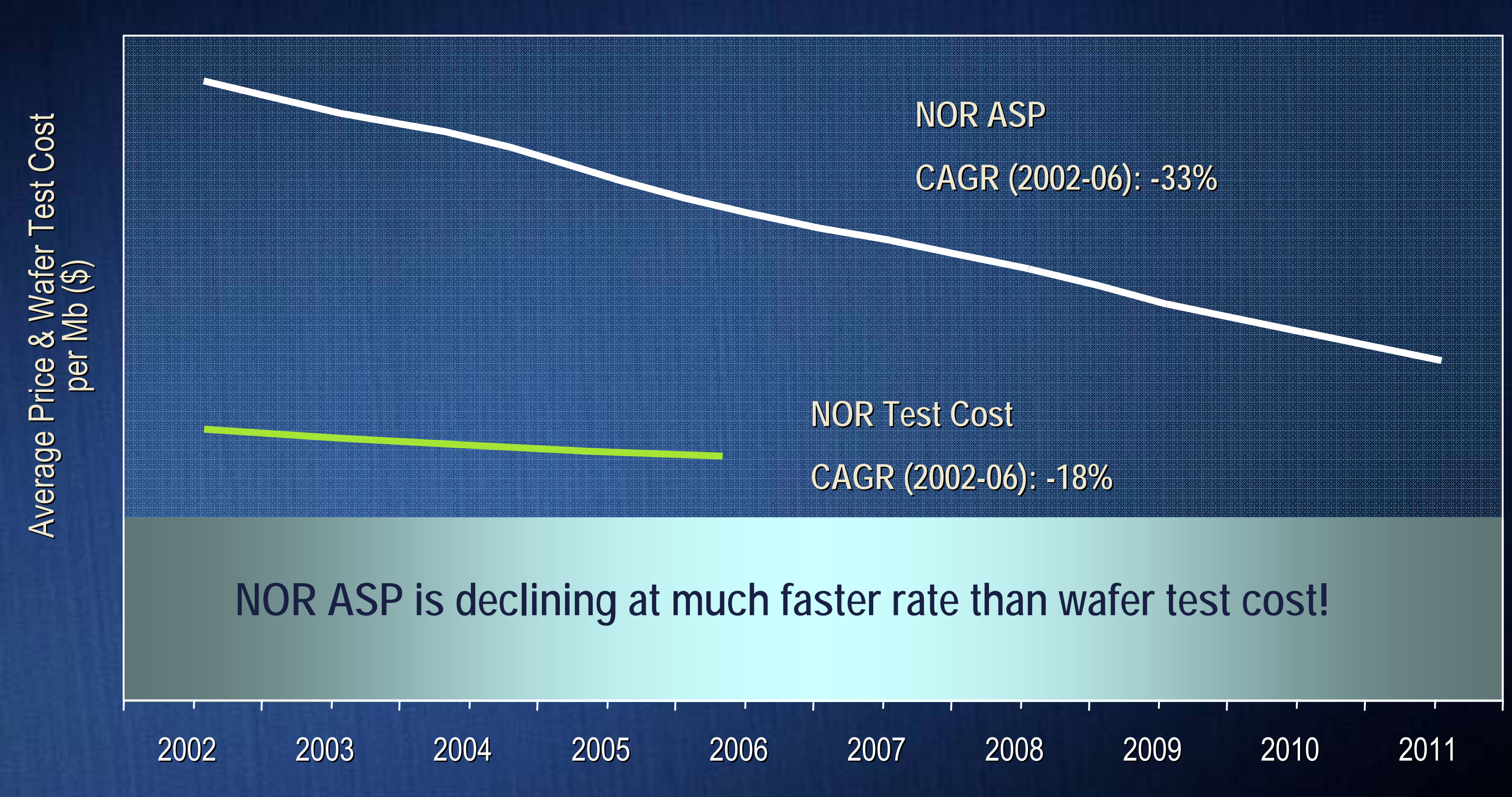
Agenda

- Wafer Test Cost Crisis
- Opportunities for Test Innovation
- Case Study
  - Proposed Test Flow Repartitioning
  - Assumptions
  - Scenario 1: Reduce Package Cost
  - Scenario 2: Reduce Test Cost
  - Scenario 3: Improve Product Yield
  - Case Study Summary
- Conclusions

Wafer Test Cost Crisis
Dangerous trend in device ASP and test cost



**Source: Gartner & FFI Marketing*

Wafer Test Cost Crisis

Cost challenges lead to industry consolidation

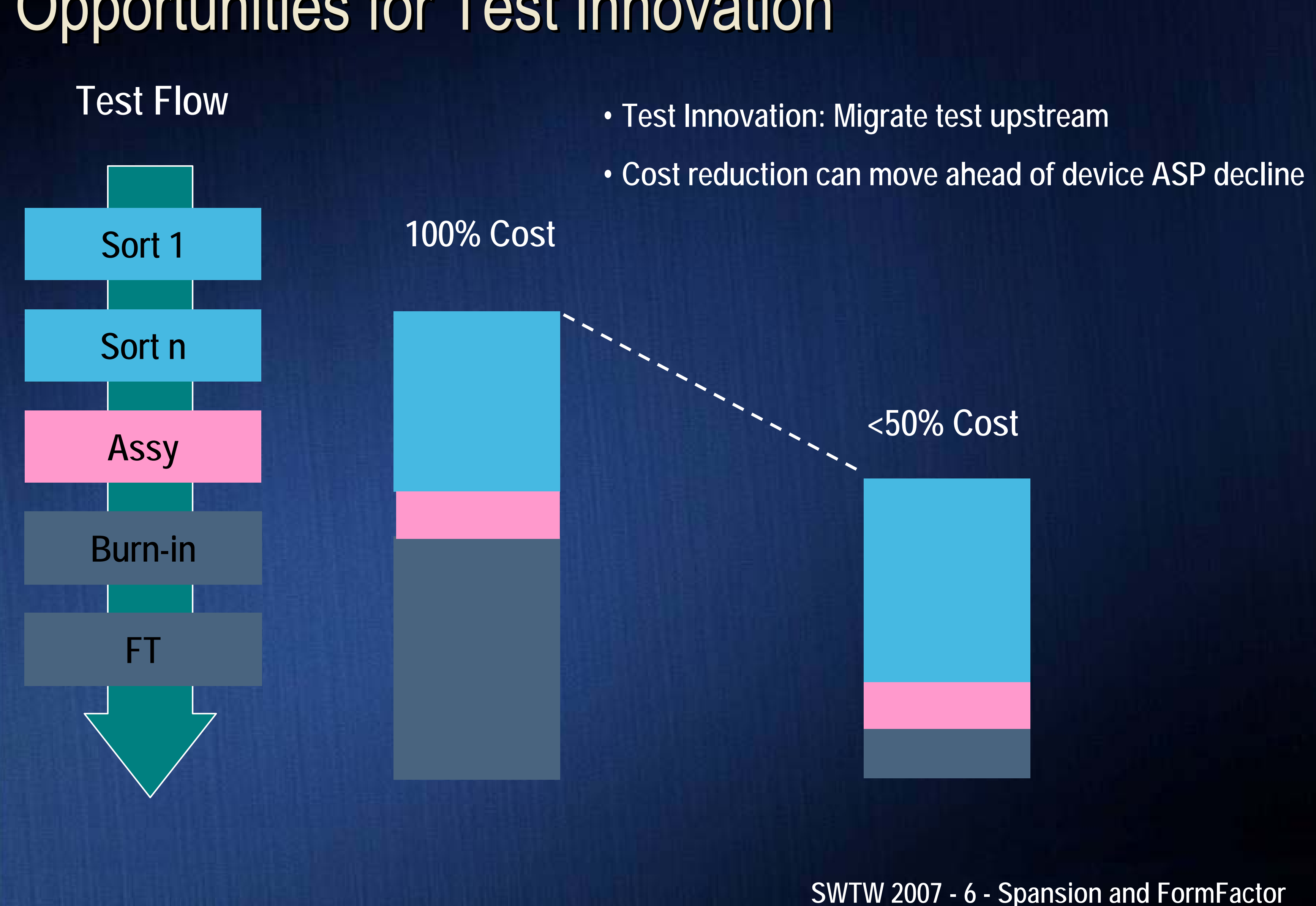
	2004	2007	2010
1	SPANSION	SPANSION	SPANSION
2	intel	intel	SAMSUNG
3	ST	ST	[intel ST] ?
4	SHARP	SAMSUNG	?
5	RENESAS	RENESAS	
6	TOSHIBA	SST	
7	SAMSUNG		
8	SST		
9	MXIC		
10	ATMEL		

**Source: Gartner & FFI Marketing*

Wafer Test Cost Crisis

CHINESE CHARACTERS FOR *"CRISIS"*

Opportunities for Test Innovation



Case Study

Proposed Test Flow Repartitioning

Typical Test Flow

SORT 1	SORT 2	PKG'ING	PKG BI	FINAL TEST

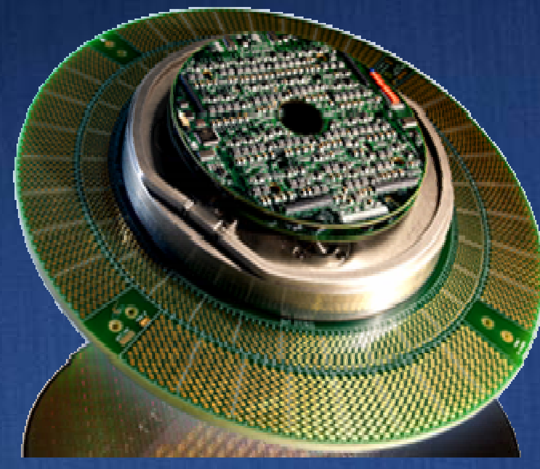
Proposed Test Flow

BURN-IN	SORT TEMP 1	SORT TEMP N	@ SPEED TEST	PKG'ING	PKG BI	FINAL TEST

Case Study
Probe Card Products

Wafer Level BI

At speed Test



FFI UPStream Probe Card

FFI High Frequency Probe Card (HFTAP)

Case Study
Assumptions

- Die/200mm Wafer Eqv: 800 dpw
  - Typical Devices: 70nm 512Mb DDR2, 90nm 256Mb NOR
- Run Rate: 100,000 wspm (200mm eqv.)
  - Typical 300mm fab maximum capacity: ~40-45k WSPM
- Yield Assumptions:
  - 95% Wafer Test Yield
  - 95% Package Yield
  - 98% Final Test Yield

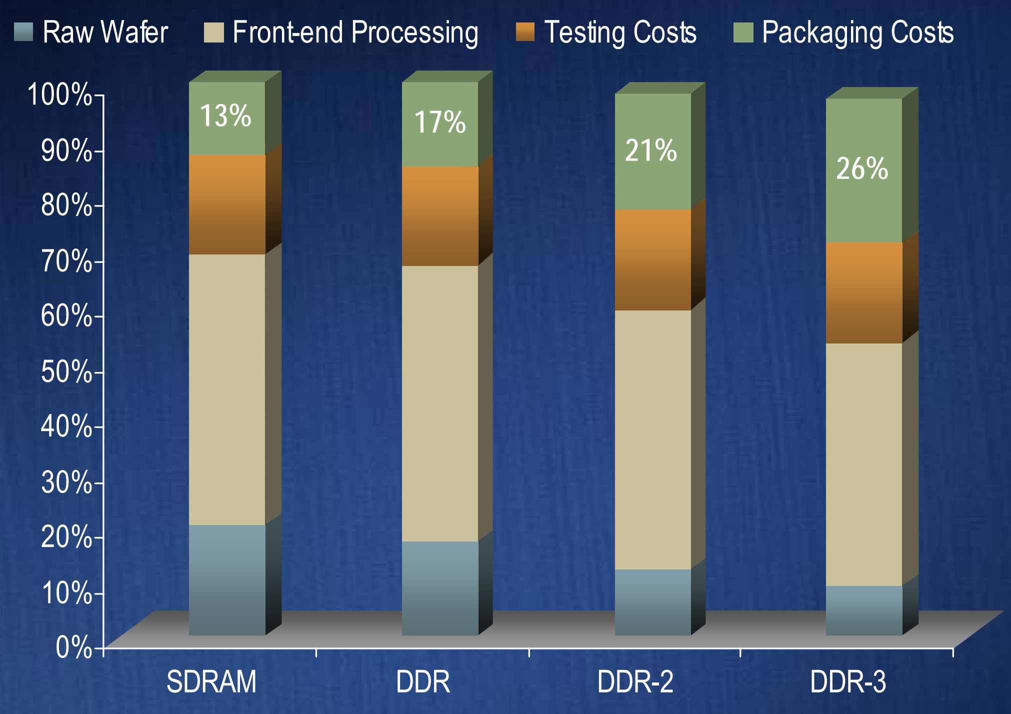
Scenario 1: Reduce Package Cost

Scenario 1: WLBI eliminates more non-repairable dies

- Save package cost for the non-repairable dies

Scenario 1: Reduce Package Cost

Wafer Test Opportunity to Reduce Packaging Cost



- Increasing packaging cost as % in product cost
- ***1% wasted package = $12M annual revenue loss***
  - BGA: -> $1 per unit
  - 300 Million Units/Qtr

**Source: Gartner & FFI Marketing*

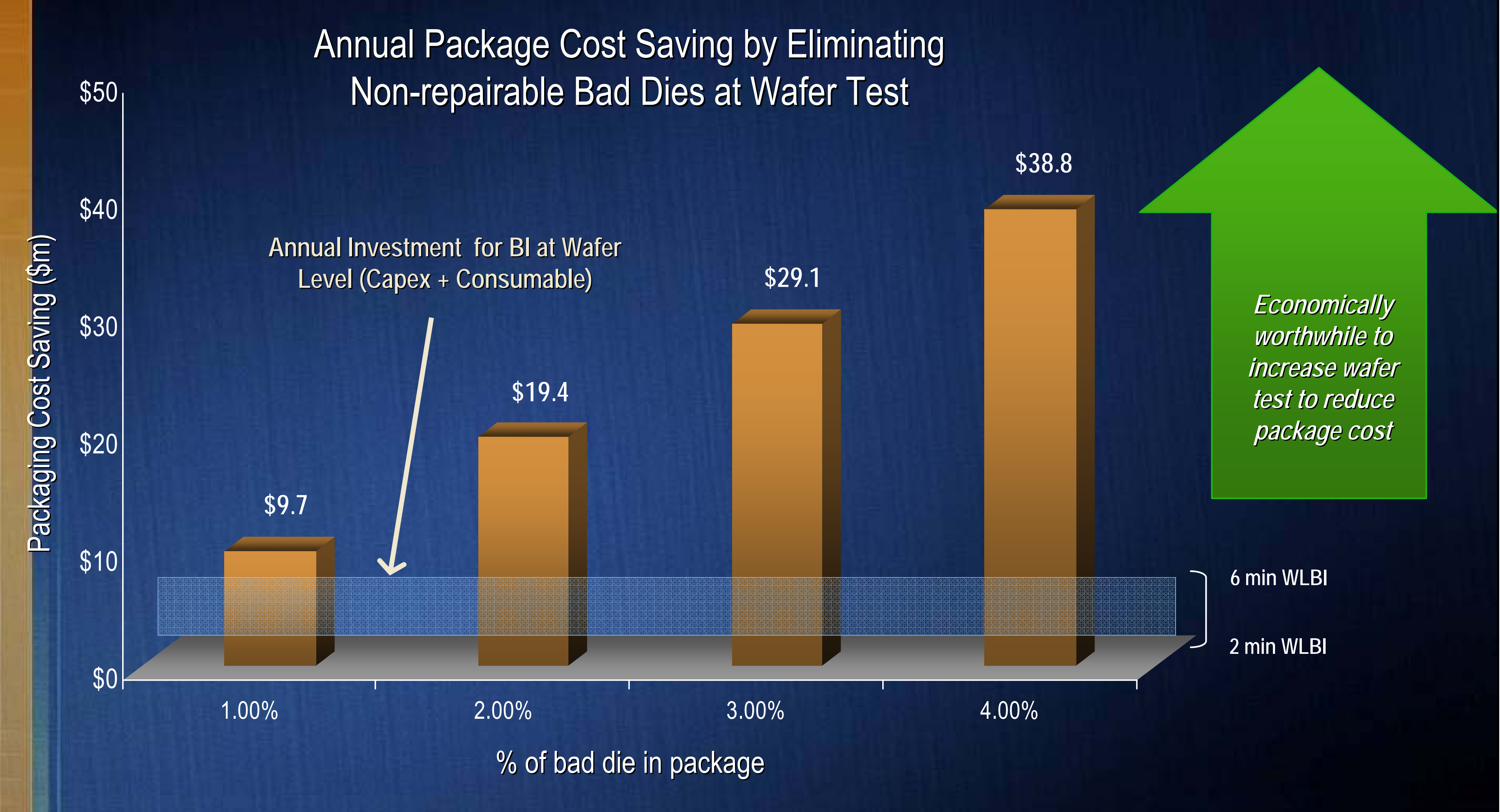
Scenario 1: Reduce Package Cost
Trade-off Questions

Question: But I have to spend more $ on wafer test Capex and probe card. How does it compare to the package cost saving?

Answer is …

Scenario 1: Reduce Package Cost

Packaging Cost Saving vs. Increased Wafer Test Investment



Scenario 2: Reduce WLBI Test Cost

Introduce High Temp BI at Wafer Level

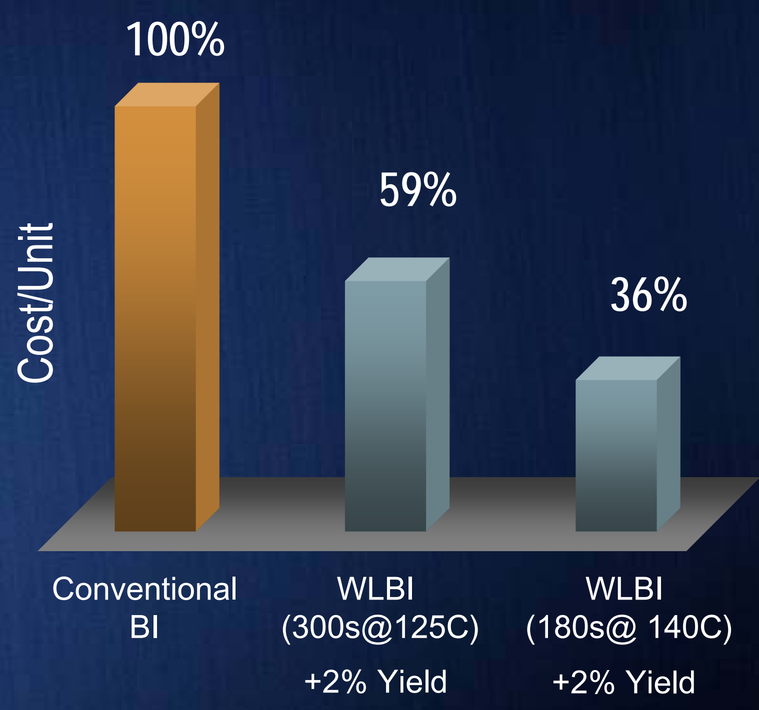
Case 2: Add High temperature WLBI to reduce BI cost

- Reduce package BI time
- Detect more early life failures
- Earlier and more data for feedback to Fab

Scenario 2: Reduce WLBI Test Cost

BI Test Cost Reduction

- Decreased total test cost
  - 41% with WLSBI @ 125°C
  - 64% with WLSBI @ 140°C
- Increased yield
  - 2% yield increase after package BI
- Reduced package BI time
  - BI time cut in half with 140°C



Scenario 2: Reduce WLBI Test Cost

Trade-off Questions

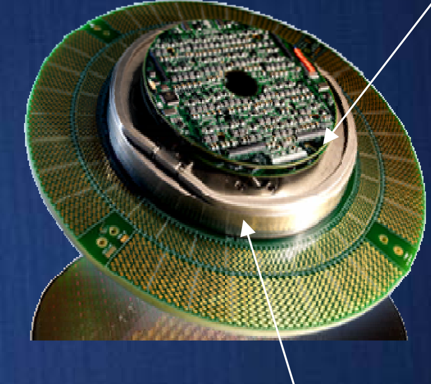
Question: Can the probe card work reliably at high temperature in production environment?

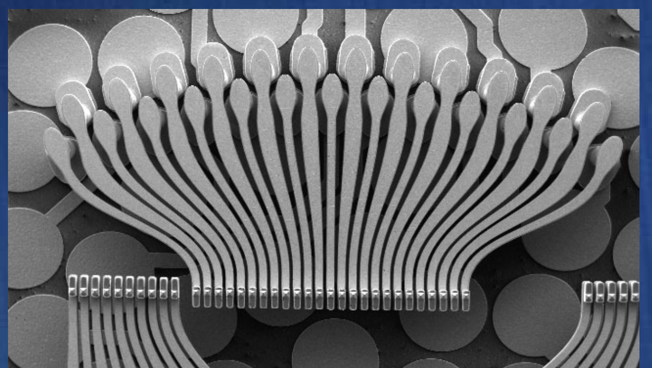
Answer is …

Scenario 2: Reduce WLBI Test Cost
High Temperature BI Probe Card

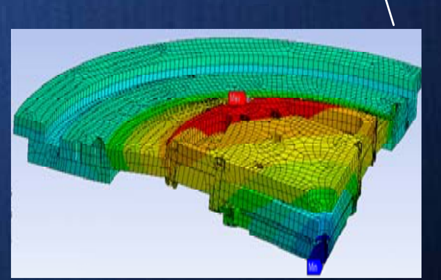
- WLBI probe card needs to be optimized for
  - High temperature
  - High parallelism
  - Low pad damage

Selection of high temperature electronic component





MicroSpring™ optimized for tight pitch at high temperature



FFI proprietary thermally optimized system for stable planarity at high temperature

Scenario 3: Improve Product Yield
Migrate Partial Final Test to Wafer Level

- Scenario 3: Moving some final test to wafer
  - Detect and repair more dies to improve product yield
  - Higher probing temperature to replicate final test conditions
  - At speed test to validate device performance

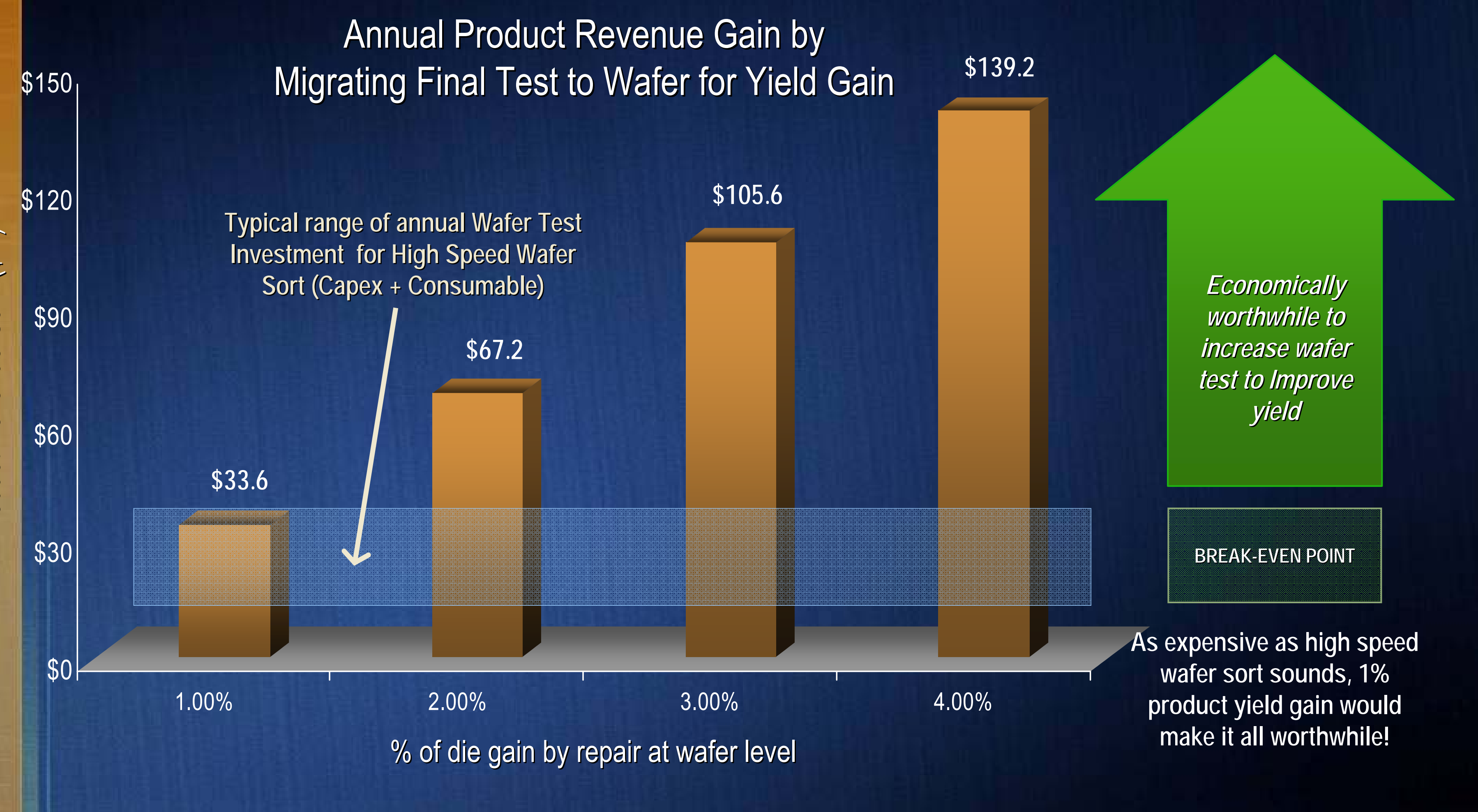
Scenario 3: Improve Product Yield
Trade-off Questions

Question: High speed testers are very expensive. How much yield gain do I need to make it worthwhile?

Answer is …

Scenario 3: Improve Product Yield

Yield Gain vs. Increased Wafer Test Investment



Scenario 3: Improve Product Yield
Trade-off Questions

Question: Will high frequency sort work in high parallelism? Where are the limits?

Answer is …

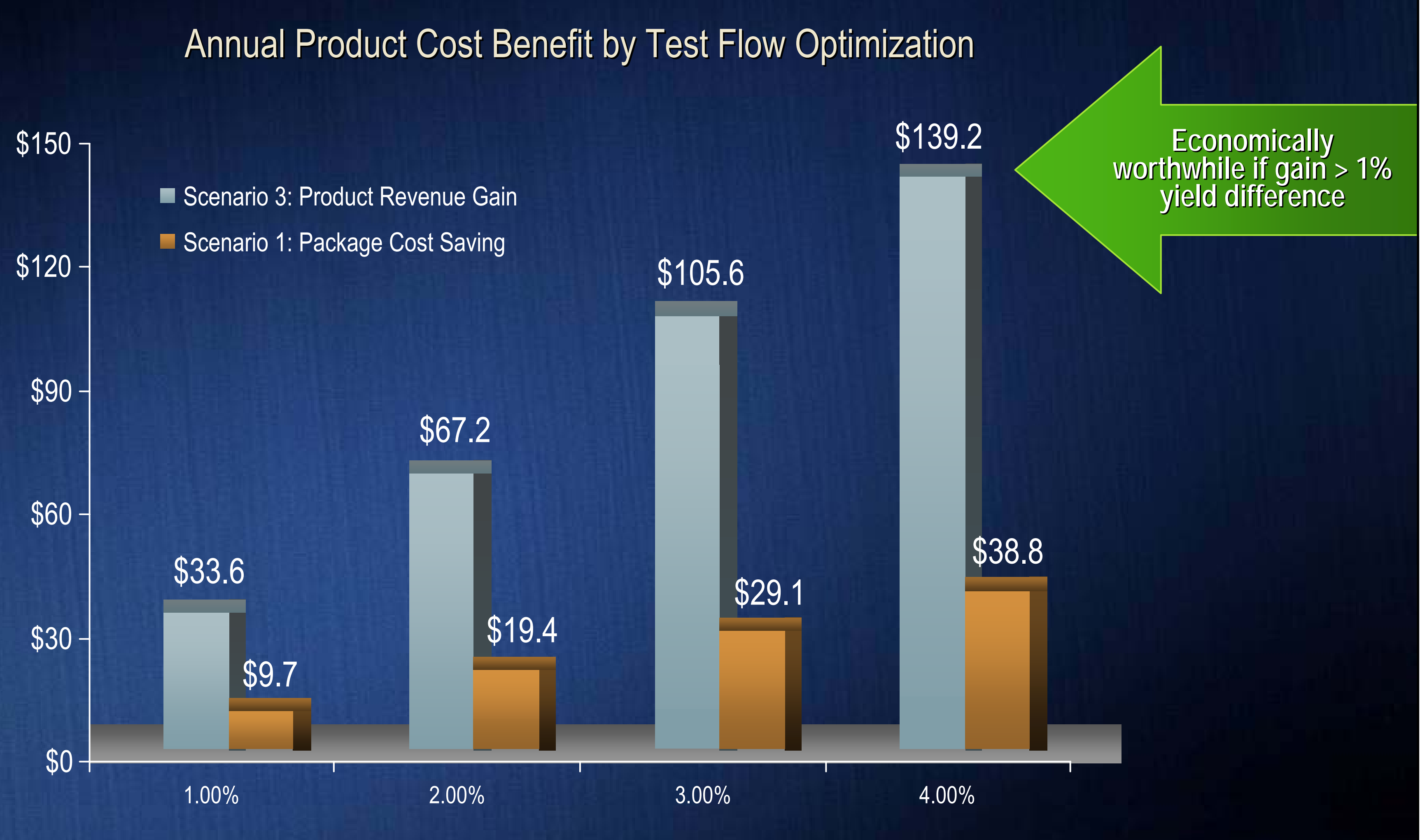
Scenario 3: Improve Product Yield
Trade-off Questions

Question: Will high frequency sort work in high parallelism? Where are the limits?

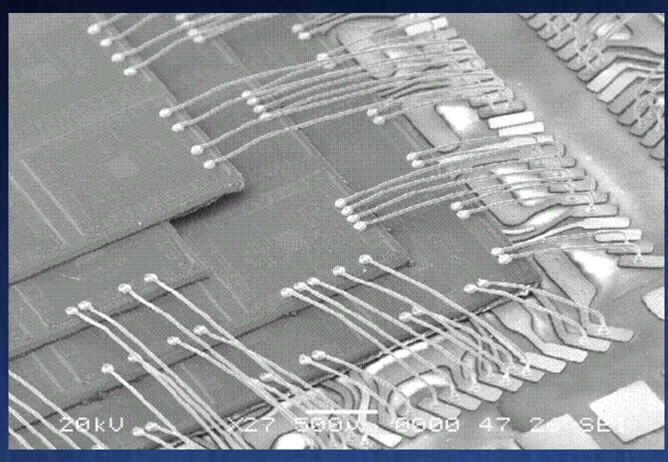
- Answer …
  - Simulations look promising
  - FFI has proven expertise on high frequency probing
    - Demonstrated x2 TRE @ 100MHz (SWTW Paper 2004)
    - Demonstrated up to 500MHz for non TRE
  - So there is only one way to find out whether it works: *Try it!*
  - The benefits are there, go for them!

Case Study Summary

Economics Benefits

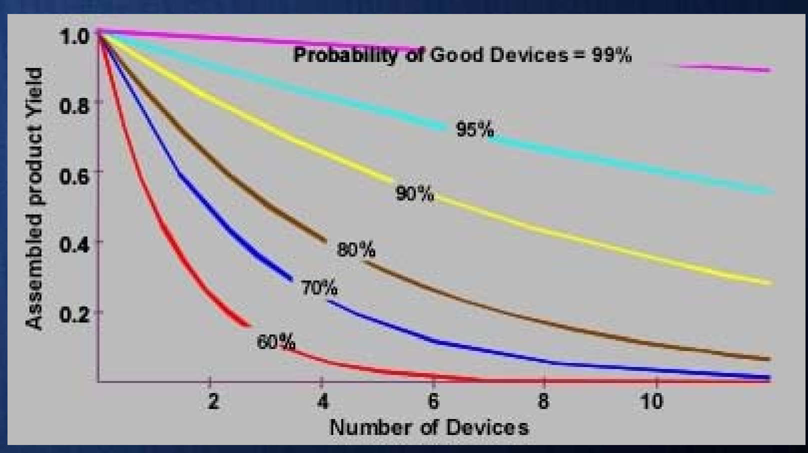


Case Study Summary
Economics Benefits for MCP



Picture of Multi-chip-package (MCP)

- Economic benefits for MCP will be even bigger!
- 1% yield delta for single chip = 5% yield delta for 5-die MCP



MCP Yield Curve vs. Single Die Yield

Conclusions

- Memory device market price pressure calls for test innovation to reduce product cost
- Migrating test upstream can provide earlier feedback for improved yield and down-stream manufacturing cost savings for the non-repairable device on wafer
- The incremental increase in wafer test spending can be easily justified if >1% yield difference is realized
- The benefits are there, go for them!