High Speed Control Bus for Advanced TRE™

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San Diego, CA  USA
Outline

- Challenges with most advanced DRAM probe cards
  - Trends in parallel test
  - Test methods to increase parallel test
  - Increased usage of Advanced Tester Resource Enhancement (A-TRE)
- Need for higher integration – customized IC development
- Control methods of Advanced TRE
- Standardization
Trends in Parallel Test of DRAM

- Parallel test has increased significantly in the last 10 years
  - Test cost and cycle time reduction
- Test times are long and are increasing with memory density
- Touchdown count has increased
- Increase of parallel test is the most efficient way to reduce test cost and cycle time
Trend in Parallel Test of DRAM

<table>
<thead>
<tr>
<th>Tester Sites</th>
<th>16</th>
<th>32</th>
<th>64</th>
<th>96</th>
<th>64</th>
<th>96</th>
<th>96/128</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallelism</td>
<td>16</td>
<td>32</td>
<td>256</td>
<td>384</td>
<td>512</td>
<td>768</td>
<td>~1000</td>
</tr>
<tr>
<td>Signal TRE</td>
<td>x1</td>
<td>x2</td>
<td>x4</td>
<td>x4/x6</td>
<td>x8</td>
<td>x6/x12</td>
<td>x8/x16</td>
</tr>
<tr>
<td>DFT</td>
<td>No</td>
<td>I/O compr.</td>
<td>I/O compr.</td>
<td>I/O compr.</td>
<td>I/O and control</td>
<td>I/O and control</td>
<td>I/O and control</td>
</tr>
<tr>
<td>A-TRE</td>
<td>none</td>
<td>none</td>
<td>none</td>
<td>none</td>
<td>none</td>
<td>DC-TRE PPS-TRE</td>
<td>DC-TRE PPS-TRE</td>
</tr>
</tbody>
</table>

- Which other capability will be needed in the future to get to the next step?
- Test time impact is very much in focus
Advanced TRE (Tester Resource Enhancement)

- TRE in the past was limited to control signals = signal TRE
  - One tester driver controls multiple DUTs

- Advanced TRE is expanding TRE to different classes of signals like DC-signals and Power supplies

- Example: DC-signals
  - DC-signals are used to force voltages - trimming
  - DC-signals are used to measure voltages - characterization
    - High accuracy is needed
  - DC-signals are more critical with regard to process related failures than control signal

*More capable TRE technology is needed*
DC-Boost™ - A DC-Signal Sharing Solution

Adding a new degree of intelligence to our wafer probe cards

- First custom designed TRE chip
- Enables TRE on DC-signals:
  - One tester channel can be used for multiple DC-signals
  - Sequence control is provided for voltage measurements
    - Allow sequential measurements by connecting one signal at a time
  - Isolation capability is provided for disconnecting bad DUTs
    - Minimize yield loss
    - Increase accuracy of applied voltage levels
- Quad DC-Boost: 2nd generation version with higher integration being currently rolled-out to the market
Test Methods to Increase Parallel Test I

- Signal TRE x4
- No DC-TRE
- No PPS-TRE
Test Methods to Increase Parallel Test II

- Signal TRE x4
- DC-TRE to enable more DC-signals per DUT
- No PPS-TRE
Test Methods to Increase Parallel Test III

- Signal TRE x8 (up to x12 for even higher parallelism)
- DC-TRE
- PPS-TRE
Increased Usage of Advanced TRE

- Number of switches is increasing:
  - Increase in DUT count
  - More DCs per DUT

Commercial parts have a very limited shrink roadmap

Custom IC shrink roadmap will support increase in switch count

- DC Boost™
- Quad DC-Boost™
- Next custom chip design

- DC-TRE channels per probe card
  - 2008
  - 2009
  - 2010
  - 2011

- Area per switch
  - 2008
  - 2009
  - 2010
  - 2011
Need for Higher Integration – Customized ICs

- Probe cards have special requirements
  - Small foot print, small area per switch
    - Ensure feasibility of highest switch count designs
    - Avoid daughter cards to increase reliability
  - High temperature: With chuck temperatures up to 125°C the components on the probe card are exposed to high temperatures
  - Package and pin assignment optimized for easy routing of the PCB
  - Special functions or combinations of features unique to IC test
  - Easy and fast control
    - Limited number of control channels
    - No test time impact due to switch operation
    - Lowest possible routing effort on the PCB
- Wide control bus using one control channel per switch
  - Limited by the number of available control channels
  - Creates significant routing problem
Control Methods for A-TRE: FFI Approach

- A-TRE controller on the probe card is controlling DC-Boost
- ProbeBus™ Technology: High speed control bus for all A-TRE chips on the probe card
- FormBus™ Technology: Communication between the test program and the A-TRE controller
Control Methods for A-TRE – FormBus™

- FormBus™: Communication between the tester and A-TRE controller
  - Wider bus (typical 18 bit) using tester control channels or
  - Very narrow (4 bit) bus using high speed tester channels:
    - Scalable to increasing switch count
    - Scalable to increasing data traffic coming with additional functionality:
      - Data read back
      - More complex control requirements
Control Methods for A-TRE – ProbeBus™

- **ProbeBus™**: High speed control bus for all A-TRE chips
  - Allow full control as well as data read back
  - Bus is designed for optimized routing of the PCB
  - DC-Boost and other future A-TRE chips can use this bus standard structure

- The A-TRE controller takes care of all data management and provides an easy interface to the test through the FormBus
  - Minimizing the programming effort and the data traffic between tester and probe card
Standardization Efforts

- Probe card with this level of complexity requires a significant amount of engineering

- Standardization of core components is a must to meet cycle time, resource and cost targets
  - Design – use standard components and placement schemes
  - Verification and outgoing test – use standard testers for outgoing test
    - Commercially available probe card testers cannot perform that function
  - Standard communication between tester and probe card are highly desirable
Standardization Efforts - User Requirements

- Different customers have very different test strategies
  - Different implementations of A-TRE
  - Different ways of controlling A-TRE on a probe card
- The current approach provides
  - Most flexible way to respond to different requirements while keeping standards on the key components (communication protocol, controller, firmware, architecture)
  - Scalability for increasing usage of A-TRE
  - Flexibility to adopt new features
Summary

- Parallel test has continued to increase enabled by A-TRE and DFT
- Increasing use of A-TRE requires:
  - Customized A-TRE chips
  - Well thought through probe card architecture
- The presented architecture fulfills the requirements in the best possible way
- The use of standard building blocks enables:
  - Short lead time and reasonable effort for these highly complex and customized products
  - Stable design and building process – “first time right”
  - Scalability to further increase the usage of A-TRE
Acknowledgements

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