International Technology Roadmap for Semiconductors

Dave Armstrong – Advantest
Ira Feldman – Feldman Engineering
Marc Loranger - FormFactor
Overview

- Who are we?
- Why a roadmap?
- What is the purpose?
- Example Trends
- How can you help?
- Summary
ITRS Team

• **Large ITRS Team**
  – More than a 1,000 professionals
  – Over 100 companies
  – 16 Working Groups

• **Test Working Group**
  – More than 70 professionals
  – More than 45 companies

• **Three of us are presenting today**
  – Dave (Advantest) – Test TWG Chairman
  – Marc (FormFactor) - Probing Team Leader
  – Ira (Feldman Engineering) - Communications
Why a Roadmap?

• The ITRS is generated each year to report on the technological fundamentals of our industry.

• In addition, by extrapolating on the trends inherent in today’s semiconductor technology we identify disconnects and discuss possible approach to overcome these challenges.

• Through this effort we all can get a better sense of the path of least resistance and align our plans and standards in a fashion which is most likely to succeed.
What Is and What Isn’t the ITRS

What Is the ITRS
- The combined expert opinion by this team.
- The results of many different technology models.
- A “best guess” of where the industry is heading for the next 15 years.
- A highlighting of disconnects and significant challenges.

What Isn’t the ITRS
- It doesn’t implement or define Moore’s Law – it just tries to predict how things will likely trend.
- A commitment from the involved companies to do what is reported.
- Specific solutions or prescriptive.
ITRS Process

Entire Team Publishes a New Roadmap Yearly

Working Group Discusses Challenges

Sub-Team Analyzes Implications

Implications Discussed with Other Working Groups

Sub-Team Reconciles Feedback from Other Groups

Armstrong-Feldman-Loranger

June 8-11, 2014

IEEE Workshop
Test Complexity Drivers

• **Device trends**
  – Increasing device interface bandwidth
  – Increasing device integration (SoC, SiP, MCP, 3D packaging)
    • Homogenous & heterogeneous dies → functional disaggregation
  – Integration of emerging and non-digital CMOS technologies
  – Complex package electrical and mechanical characteristics
  – Device characteristics beyond one sided stimulus/response model
  – 3 Dimensional silicon - multi-die and Multi-layer
  – Integration of non-electrical devices (optical, MEMS, etc.)
  – Fault Tolerant Architectures and Protocols

• **Industry trends**
  – 450 mm wafer transition
Date = When in Production

ITRS 2013 Overview: Figure 1a A Typical Technology Production “Ramp” Curve (within an established wafer generation)
## Wafer Probe Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MPU &amp; ASIC</th>
<th>DRAM</th>
<th>NAND</th>
<th>RF &amp; AMS</th>
<th>LCD Drivers</th>
<th>CIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wirebond – inline pad pitch</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Wirebond – stagger pad pitch</td>
<td>X</td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Bump – array pitch</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O Pad Size</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Wafer Test Frequency</td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
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<tr>
<td>High Speed I/O Frequency</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
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<tr>
<td>Wirebond - Probe Tip Diameter</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Bump – Probe Tip Diameter</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Probe Force</td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td></td>
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<tr>
<td>Probe (Active) Area</td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td>X</td>
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<tr>
<td># of Probes per Touchdown</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Maximum Current / Probe</td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
<td>X</td>
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<tr>
<td>Maximum Resistance</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
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<td>X</td>
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</tbody>
</table>
Parallelism Trend

DRAM Parallelism Roadmap Changes vs. time

- Roadmap Year
  - Market data
  - Multi vendor
- 2005
- 2009
- 2011
- 2013
- 2014
- 2015
- 2016
- 2017
- 2018
- 2019
- 2020

Production Year vs. Probe Card Parallelism
SoC (MPU) Bump Pitch Trend

- Technology shift in 2012
## Prober accuracy vs. Pad size

<table>
<thead>
<tr>
<th>DRAM</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
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</thead>
<tbody>
<tr>
<td>Wirebond - inline pad pitch</td>
<td>55</td>
<td>50</td>
<td>45</td>
<td>40</td>
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<td>40</td>
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<tr>
<td>I/O Pad Size (μm)</td>
<td>X</td>
<td>Y</td>
<td>X</td>
<td>Y</td>
<td>X</td>
<td>Y</td>
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<tr>
<td>Wirebond</td>
<td>45</td>
<td>45</td>
<td>40</td>
<td>40</td>
<td>35</td>
<td>40</td>
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</table>

<table>
<thead>
<tr>
<th>Prober</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
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</thead>
<tbody>
<tr>
<td>XY Accuracy(Probe to Pad) [um]</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Z Accuracy(Probe to Pad) [um]</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Chuck Planarity [+/-um]</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
<td>7.5</td>
</tr>
</tbody>
</table>

- Prober roadmap is not tracking with decreasing pad sizes
- An especially difficult issue for Full Wafer Contactor probe cards
Next Challenges for Probe Cards

- Decreasing pad / bump sizes and pitch
- Increasing parallelism SoC and Memory
- Increased use of die for MCP, 2.5D and 3D integration will drive more wafer sort
- 2 sided probing
- Testing stacked devices (e.g. HBM)
- MEMS and sensor sort test
- Cost of test as a driver

Armstrong-Feldman-Loranger

June 8-11, 2014 IEEE Workshop
Opportunities for Involvement!

• Download ITRS data at:
  http://www.itrs.net/Links/2013ITRS/Home2013.htm

• Provide feedback on test data at:
  http://j.mp/ITRSTestSurvey

• Sign up:
  dave.armstrong@advantest.com
Summary

- **Great Tool**
  - Well accepted independent industry wide reference

- **Challenges**
  - Requires broad-based inputs
  - Track potential disruptive technology

- **Help Us**
  - Get Involved!