IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 8 - 11, 2014 | San Diego, California

International Technology Roadmap for Semiconductors

ADVANTEST

FELDMAN ENGINEERING

FORMFACTOR INC.

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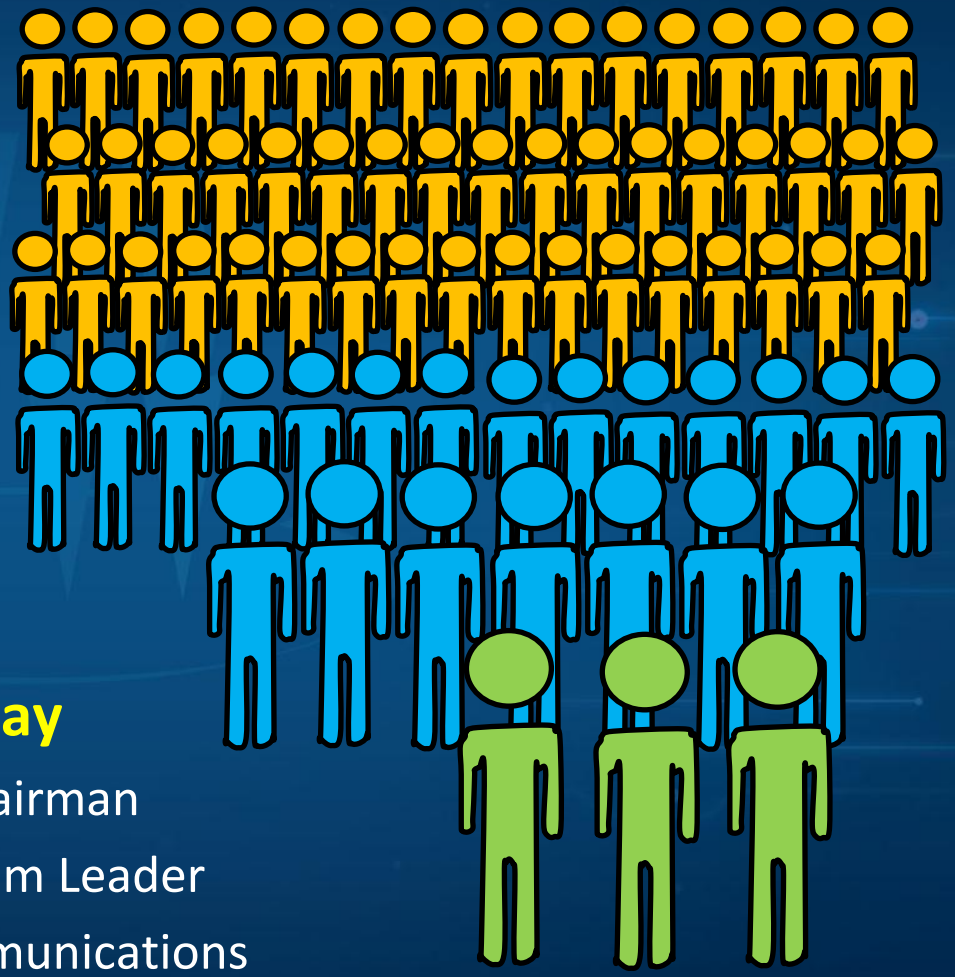
Overview

- Who are we?
- Why a roadmap?
- What is the purpose?
- Example Trends
- How can you help?
- Summary

ITRS Team

- **Large ITRS Team**
  - More than a 1,000 professionals
  - Over 100 companies
  - 16 Working Groups
- **Test Working Group**
  - More than 70 professionals
  - More than 45 companies
- **Three of us are presenting today**
  - Dave (Advantest) – Test TWG Chairman
  - Marc (FormFactor) - Probing Team Leader
  - Ira (Feldman Engineering) - Communications



Why a Roadmap?

- The ITRS is generated each year to report on the technological fundamentals of our industry.
- In addition, by extrapolating on the trends inherent in today's semiconductor technology we identify disconnects and discuss possible approach to overcome these challenges.
- Through this effort we all can get a better sense of the path of least resistance and align our plans and standards in a fashion which is most likely to succeed.

What Is and What Isn't the ITRS

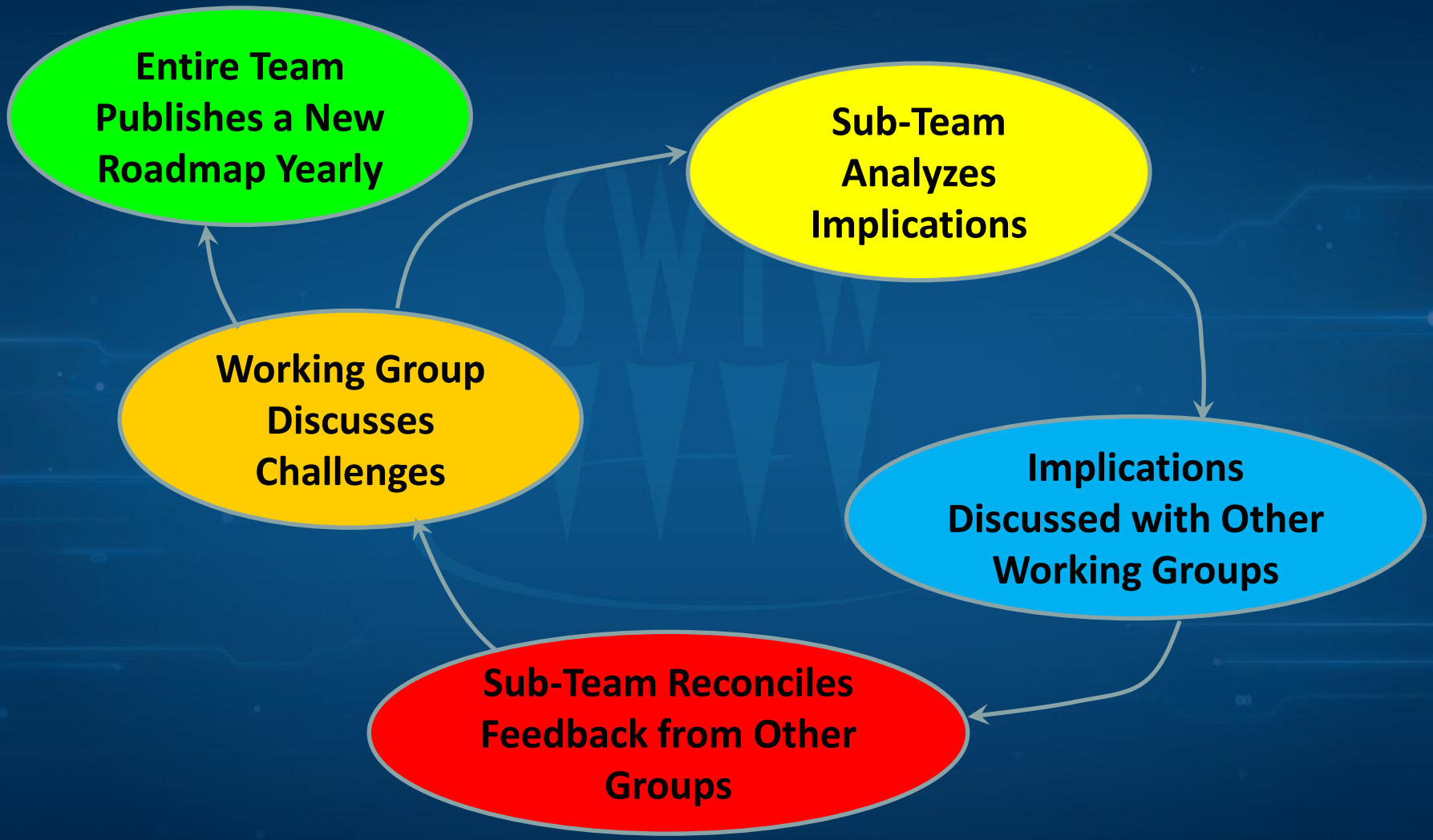
What Is the ITRS

- The combined expert opinion by this team.
- The results of many different technology models.
- A "best guess" of where the industry is heading for the next 15 years.
- A highlighting of disconnects and significant challenges.

What Isn't the ITRS

- It doesn't implement or define Moore's Law – it just tries to predict how things will likely trend.
- A commitment from the involved companies to do what is reported.
- Specific solutions or prescriptive.

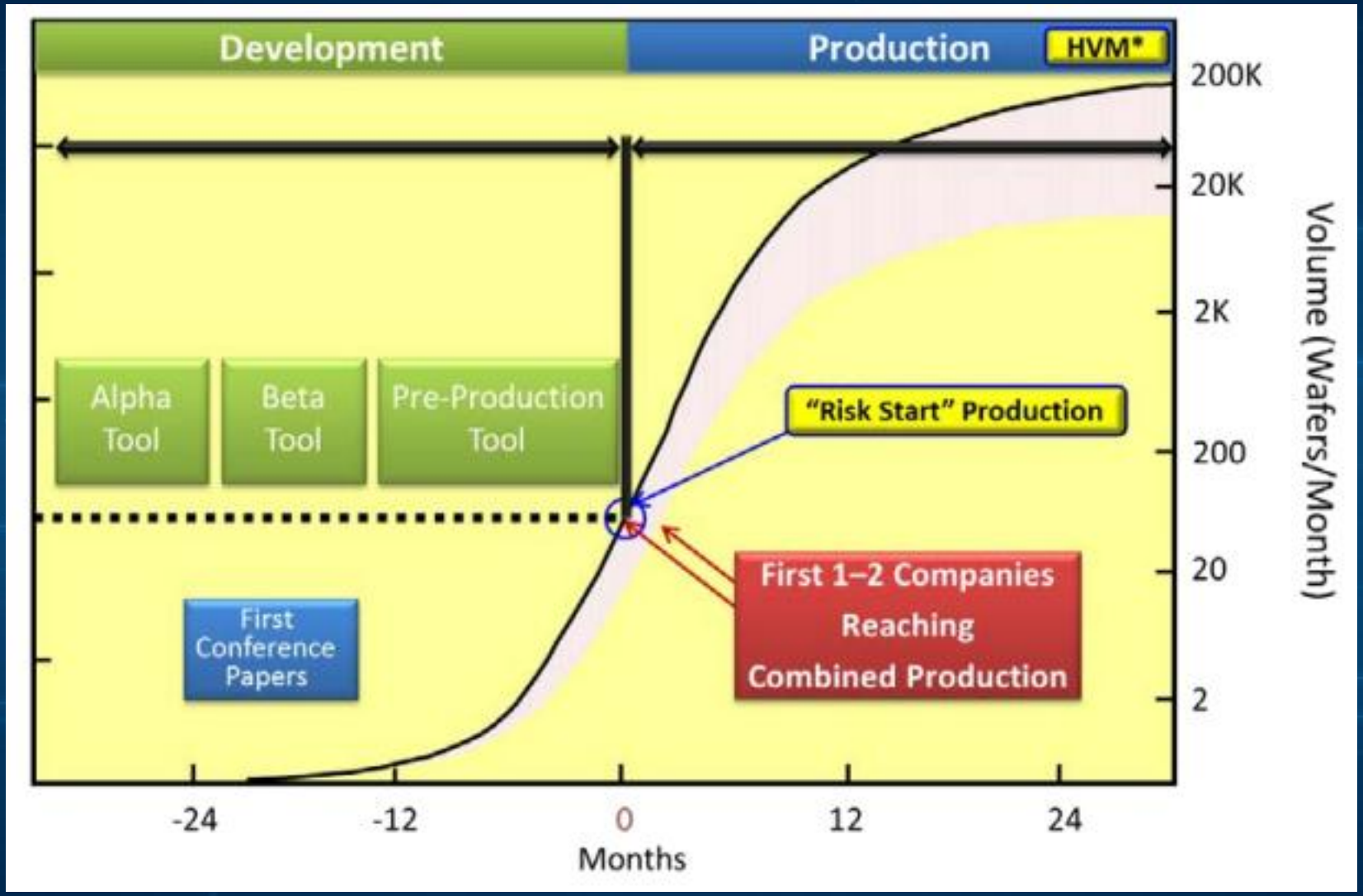
ITRS Process



Test Complexity Drivers

- **Device trends**
  - Increasing device interface bandwidth
  - Increasing device integration (SoC, SiP, MCP, 3D packaging)
    - Homogenous & heterogeneous dies → functional disaggregation
  - Integration of emerging and non-digital CMOS technologies
  - Complex package electrical and mechanical characteristics
  - Device characteristics beyond one sided stimulus/response model
  - 3 Dimensional silicon - multi-die and Multi-layer
  - Integration of non-electrical devices (optical, MEMS, etc.)
  - Fault Tolerant Architectures and Protocols
- **Industry trends**
  - 450 mm wafer transition

Date = When in Production

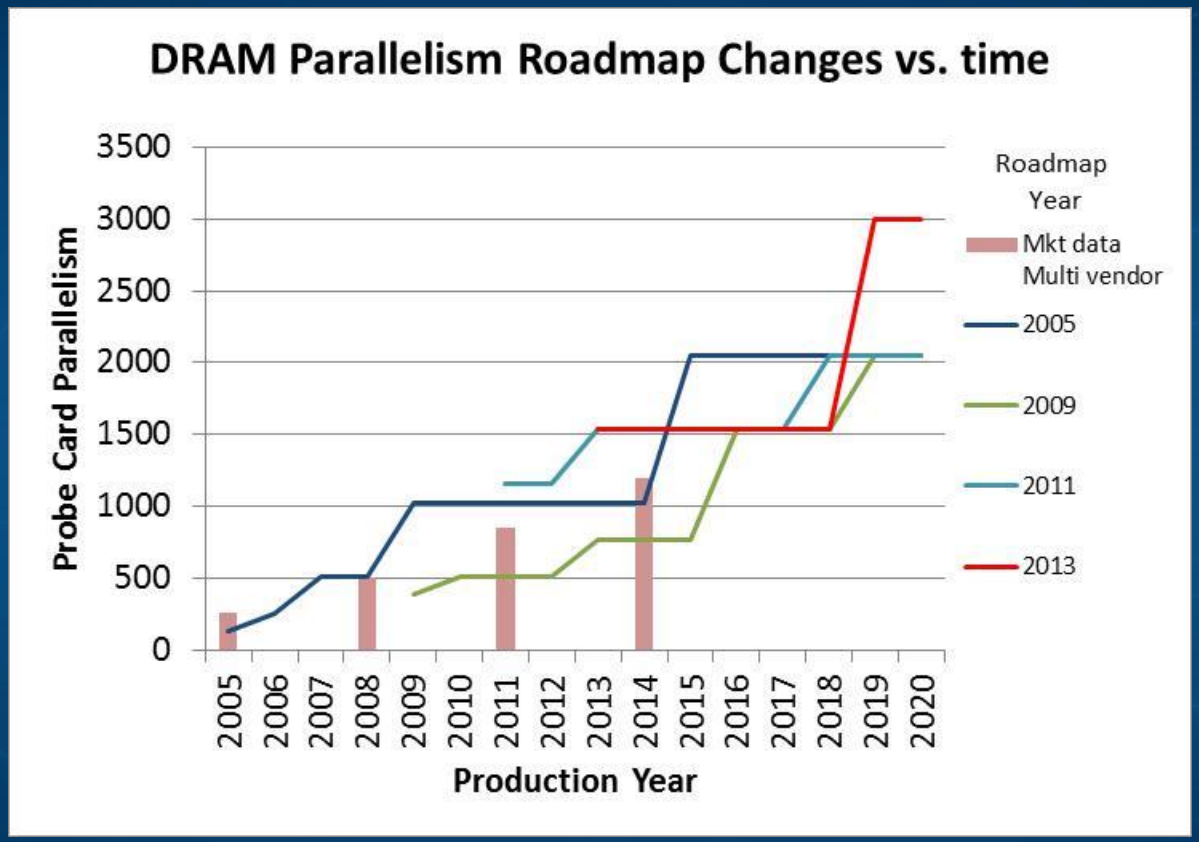


ITRS 2013 Overview: Figure 1a A Typical Technology Production "Ramp" Curve (within an established wafer generation)

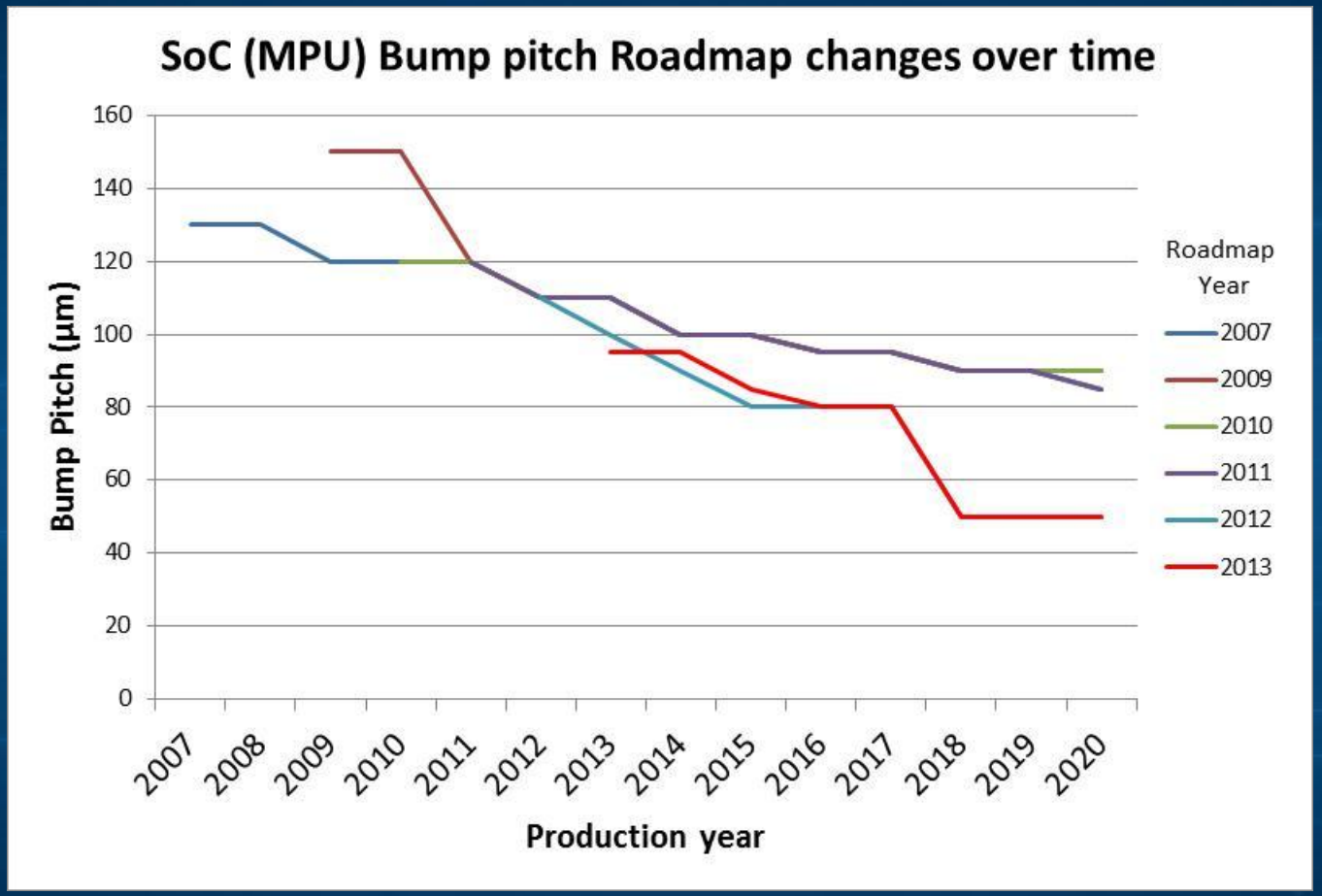
Wafer Probe Requirements

Parameter	MPU & ASIC	DRAM	NAND	RF & AMS	LCD Drivers	CIS
Wirebond – inline pad pitch	X	X	X	X	X	X
Wirebond – stagger pad pitch	X			X	X	
Bump – array pitch	X			X		
I/O Pad Size	X	X	X	X		X
Wafer Test Frequency	X	X	X			X
High Speed I/O Frequency	X				X	X
Wirebond - Probe Tip Diameter	X	X	X	X	X	X
Bump – Probe Tip Diameter	X			X		
Probe Force	X	X	X		X	X
Probe (Active) Area	X	X	X	X	X	X
# of Probes per Touchdown	X	X	X	X	X	X
Maximum Current / Probe		X	X	X	X	X
Maximum Resistance		X	X		X	

Parallelism Trend



SoC (MPU) Bump Pitch Trend



- **Technology shift in 2012**

Prober accuracy vs. Pad size

	2013		2014		2015		2016		2017		2018	
DRAM												
Wirebond - inline pad pitch	55		50		45		40		40		40	
I/O Pad Size (µm)	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
Wirebond	45	45	40	45	40	40	35	40	35	40	35	40
Prober												
XY Accuracy(Probe to Pad) [um]	2.0		2.0		2.0		2.0		2.0		2.0	
Z Accuracy(Probe to Pad) [um]	5.0		5.0		5.0		5.0		5.0		5.0	
Chuck Planarity [+/-um]	7.5		7.5		7.5		7.5		7.5		7.5	

- **Prober roadmap is not tracking with decreasing pad sizes**
- **An especially difficult issue for Full Wafer Contactor probe cards**

Next Challenges for Probe Cards

- Decreasing pad / bump sizes and pitch
- Increasing parallelism SoC and Memory
- Increased use of die for MCP, 2.5D and 3D integration will drive more wafer sort
- 2 sided probing
- Testing stacked devices (e.g. HBM)
- MEMS and sensor sort test
- Cost of test as a driver

Opportunities for Involvement!

- **Download ITRS data at:**

  http://www.itrs.net/Links/2013ITRS/Home2013.htm

- **Provide feedback on test data at:**

  http://j.mp/ITRSTestSurvey

- **Sign up:**

  dave.armstrong@advantest.com

Summary

- **Great Tool**
  - Well accepted independent industry wide reference
- **Challenges**
  - Requires broad-based inputs
  - Track potential disruptive technology
- **Help Us**
  - Get Involved!